# Design 08-064

作品名稱

## 高效能 JPEG XR 編解碼器

High performance JPEG XR CODEC

隊伍名稱

**Revolution**

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## 作品摘要

快速發展的感測器、顯示裝置、運算引擎與有效的演算法與架構，使得影像無所不在，過去幾年，JPEG已經融入了我們的生活，像是數位相機、部落格等等，但JPEG所能提供的影像品質有限，在2006年，新的JPEG XR影像壓縮標準已經提出並且在此討論與使用VLSI架構去實現。JPEG XR擁有相當高的編碼效率與豐富的編碼功能，在相同壓縮倍率下，更能提供與JPEG2000相似的影像品質

本作品中，會對JPEG XR編碼器進行演算法分析與提出新的硬體架構，除此之外，4 : 4 : 4的HD影像可以順利編碼，在JPEG XR編碼器中，熵編碼是整個編碼器的核心，這部份是數學運算最複雜的地方，所以我們第一個提出的技巧就是在熵編碼時，使用管線排程的方式來增加執行速度與產出量，另外的所提出的架構就是在前置濾波器與PCT，為了最佳化這部份與充分的利用矽晶圓的單位面積，我們提出資料重複技術來解決這問題，此技術可以節省對外部記憶體存取的頻寬達33%，其它還有很多的架構來節省面積與增加編碼效率。

我們藉由元件庫設計方式實做一顆JPEG XR編碼器，實際模擬結果，我們提出的架構可以執行每秒34.1百萬樣本的編碼器，這顆IC可以廣泛的應用在數位影像上，並且是低運算複雜度、低儲存空間與高動態範圍的一顆影像壓縮晶片。

## Abstract

With rapid progress of sensors, display devices, computing engines, and efficient algorithm/architecture, image application exists everywhere. In the past years, JPEG is well-know image compression standard. It has been merged together with our life such as digital still camera, blog and others. But JPEG can't satisfy the rapid progress of technology. For satification of the high quality image compression, the new JPEG XR compression algorithm is discussed and implemented with the VLSI architecture. JPEG XR has high encoding efficiency and versatile functions. The image quality of JPEG XR is nearly equal to JPEG 2000 with the same bit-rate.

The analysis and architecture design of JEPG XR encoder are also proposed in this work. Besides, the 4:4:4 high definition photo can be encoded in smooth. In JPEG XR encoder, Entropy coding is the heart of encoder. Therefore, we first proposed a timing schedule of pipeline architecture to speed up the entropy encoding, which is the most computationally intensive part in JPEG XR encoder. Another improved architecture in this work is the optimization of Pre-filter and PCT. To optimal this problem and maximize the silicon area efficiency, we also proposed a data reuse skill to solve this problem. The data reuse skill can reduce 33% memory bandwidth form external memory. There are many architecture to reduce the hardware cost under the same throughput.

A baseline JPEG XR encoder has been implemented by cell-based IC design flow. According to the simulation results, the throughput of the proposed design can encode 34.1 M samples/sec. This design can be used for the digital photography applications to achieve the low complexity of computation, low storage, and high dynamic range.