Design 08-101

作品名稱

一個快速鎖定兼具低功率消耗特性的5.5-GHz頻率合成器

A 5.5-GHz Low-Power Fast-Locking Frequency Synthesizer

隊伍名稱

為了部落 For BL

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作品摘要

由於資訊網路的加速發展，無線通訊系統因而蓬勃興起，然而因應更多不同的應用與需求，頻寬與速度的限制考量更為重要，尤以在無線行動通訊系統當中，電路的耗能將因為電路的高頻處理速度備受考驗，對於適攜性之行動通訊產品而言，高功率消耗意味使用時間與待機時間的縮短，於市場需求上，將會需求更昂貴先進的儲能裝置，致使成本增長；此外，於通訊系統的應用中，為了避免影響鄰近通道的訊號，通常也會對鄰近通道的頻率突波(Sideband Spur)大小有著一定的限制，而這個雜訊來源通常是來自於參考頻率突波(Reference Spur)。因此，更高的頻寬與速度，並且可以有效降低耗能，以及能夠有效壓抑參考頻率突波，是當今市場競爭的需求與科技研究上的議題。

此次設計中，我們加入了加速鎖定之電路，藉由這個電路，可以在適當時機改變鎖相迴路之頻寬，以達到較快速的鎖定時間，並且不會犧牲掉有效抑制雜訊與參考頻率突波的優點。在低功率的設計考量上，我們創新設計了兩個除頻器電路，以取代傳統的數位除頻器電路或電流模式邏輯(Current Mode Logic, CML)除頻器電路，其中在前端的數位除頻器電路可以操作在較真實單一相位時脈(True Single Phase Clock, TSPC)除頻器遭小的輸入電壓振幅下，因此在不同的設計考量上，可以彈性降低壓控振盪器及緩衝器所需的電流消耗；中頻除頻器電路由於其架構可以減少不必要的狀態切換次數，因此可以較傳統TSPC除頻器電路有較低的功率消耗。

電路之設計與佈局皆採用TSMC 0.18μm 1P6M CMOS製程，若不包括迴路濾波器，電路含穩壓電容總面積為1.246×1.124mm2，當電路鎖定在5.48 GHz並且頻寬為40 kHz的情況時，鎖定時間約在20~25μs，改善了約60μs，整體功率消耗亦約在9 mA。

Abstract

Phase-locked loop (PLL) is employed in various applications. Among which, the PLL-based frequency synthesizers are essential components in the communication systems. In these different systems, the PLL must satisfy many design requirements to ensure a high communication quality. These requirements include phase noise, sideband spur, power consumption, frequency tuning range, VCO tuning gain, and locking/settling time etc. Tradeoffs often exist among different design specifications. For example, narrow PLL bandwidth may be required to minimize the noise contribution from the dividers and to suppress reference spurs. However, this leads to an elongated locking time. Furthermore, as the operating frequency increases, power consumption also rises. In particular, the high-frequency dividers often dominate the chip current consumption.

This work presents a PLL-based frequency synthesizer with a fast-locking capability. The PLL incorporates a proposed digital discriminator aided phase detector (DAPD) to expedite the loop settling. The DAPD enables a fast locking by sensing the input phase error to adjust the programmable charge pump and loop filter. Moreover, two digital frequency dividers, one divide-by-2 and one divide-by-4/5, are proposed to accomplish low-power and high-speed divider operation. The PLL is fabricated in a 0.18-μm CMOS process. With the proposed digital DAPD, the settling time is considerably reduced to 20 μs without sacrificing the characteristics of a 40-kHz loop bandwidth at lock. The measured 5.5-GHz PLL phase noise at 1-MHz offset is -110.9 dBc/Hz, and the reference spurs at 10-MHz offset are lower than -75 dBc. The whole PLL consumes 9 mA from a 1.8-V supply voltage, while the two high-frequency dividers consume 1.4 mA only.