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| 作品名稱 | **具晶片速度分類與校正機制的自我功能測試**<br>Speed Binning and Calibration Mechanism for On-Chip Self Functional Test |
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## 作品摘要

由於積體電路製程與設計進步，積體電路設計朝向系統化發展，而使得電路設計複雜度大幅提升，然而，積體電路的測試也面臨更多新的挑戰，測試複雜度與測試價格不斷升高，現行測試機台無法負擔新一代SoC電路測試，因此有廠商提出DFT測試機台的構想，希望DFT電路不只負責直接或者輔助測試，也可負擔部份測試機台的工作，但DFT測試機台還是無法解決其他現行測試機台遇到的問題。因此，[3]提出以無線測試平台來解決傳統測試平台的困境。其目的是藉由無線傳輸機台機制完成晶片測試，此方式可降低現行昂貴測試機台成本，已成為未來SoC測試主要趨勢。

而本篇論文主要探討利用無線測試方式進行at-speed testing，有別於傳統at-speed testing技術調整全部clock edge，我們運用傳統Scan based delay testing來進行at-speed testing，此方式亦可使用較低速的頻率提供測試向量，再利用內部電路調整單一觸發訊號來達成at-speed testing以及speed binning。

## Abstract

Advanced integrated circuit design technology can support the design of system integrated circuit (SoC). There are many test challenges generated from design of highly complex SoC, e.g. circuit delay test and performance binning. As traditionally slower ATE tester cannot support at-speed testing, thus BIST circuit is urgently required used to solve circuit speed testing related problem. In this report, an at-speed BIST testing technique is proposed. It differs from traditional circuit speed testing techniques by changing the system clock rate. This method supplies test pattern to the circuit using lower-speed clock frequency, then applies internal BIST circuit to adjust clock edge for at-speed circuit delay testing and performance binning. The self wide-range (26%~76%), fine-scale (34ps) duty cycle adjustment technique with high-precision (28ps) calibration circuit is proposed for at-speed delay test and performance binning. Test chip DFT strategies are fully validated by instruments and HOY wireless test system.