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作品名稱

高速高能量轉換效率的逐漸趨近式類比至數位轉換器

High-Speed High-Energy-Efficiency Successive-Approximation Analog-to-Digital Converters

隊伍名稱

給我金坷垃 Give Me Jinkela
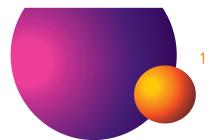
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作品摘要

目前許多無線通訊的系統(如802.11a/b/g/n)、高畫質電視接收器(HDTV receiver)等應用,皆需要一個中速(10~100 MS/s)、中高解析度(8~12 bit)的類比至數位轉換器(ADC),這樣規格的類比至數位轉換器長期由管線式(pipelined)架構所主宰。然而,目前先進製程的發展趨勢為元件的輸出阻抗和操作電壓不斷的降低,此趨勢將對於管線式架構的設計帶來更嚴重的挑戰。逐漸趨近式類比至數位轉換器(SAR ADC)相對於其他架構而言,具有較低功率消耗和低面積的潛在優勢。不過,其需要多次循環才能得到一筆完整資料,因此不利於高速的應用。然而,拜製程技術快速進步所賜,SAR ADC可操作的速度越來越快,已漸漸可以取代部分管線式類比至數位轉換器所主宰的取樣範圍。因此,我們這次的作品,將呈獻了一系列SAR ADC的設計與實作介紹,透過實際的晶片下線和量測驗證,證實所提出之電路設計技術可以有效提升電路的操作速度以及降低每次轉換所消耗的能量,比其他文獻中一流的作品有著更優異的結果。所提出的電路設計技術以及晶片實作成果簡述如下:

第一個技術為單調式的電容切換機制,其比傳統的切換方式節省約81.3%的切換能量以及50%的取樣電容。在0.13-μm CMOS製程下,我們以此技巧來實現一個10-bit,50-MS/s的SAR ADC。在1.2-V電壓下,其功率消耗為0.826 mW,有效位元為9.18 bit,等效的FOM僅為29 fJ/conversion-step。

第二個技術為二進制的錯誤補償機制。高速操作的SAR ADC,由於每個位元週期的時間非常短,常常在DAC電壓還沒穩定的時候就必須要做下一次的比較,DAC電壓穩定的問題嚴重影響電路的效能,也限制了電路的操作速度。我們提出了一個二進制的錯誤補償機制,讓比較器可以在DAC還沒穩定的時候先做比較,以提升電路操作速度。在65 nm CMOS製程下,我們利用此技巧來實現一個10-bit,100-MS/s的 SAR ADC。在1.2-V電壓下,其功率消耗為1.13 mW,有效位元為9.51 bit,等效的FOM僅為15.5 fJ/conversion-step。

第三個技術則是利用一個輔助預測電路,來避免不必要的電容切換,此技術可以省下40-45%的電容切換能量消耗。配合第一個技術,電容切換的能量消耗比傳統方法減少約90%。除此之外,這個技術還能改善電路的靜態以及動態效能。在0.18-μm CMOS製程下,我們利用此技巧來實現一個10-bit,10-MS/s的SAR ADC。在1-V電壓下,其功率消耗僅為98 μW,有效位元為接近理想的9.83 bit,等效的FOM僅為11 fJ/conversion-step。

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Abstract

An analog-to-digital converter (ADC) with a medium sampling rate (10~100 MS/s) and a medium resolution (8~12 bit) is a necessary building block for 802.11/a/b/g/n wireless networks and digital TV applications where pipelined ADCs are extensively used. However, the pipelined architecture requires several operational amplifiers, which results in large power dissipation. Moreover, the restrictions for advanced CMOS processes make high performance amplifier design challenging. However, in successive-approximation register (SAR) architectures, the conversion time and power dissipation become smaller with the advancement of CMOS technologies. Since SAR ADCs take advantage of technological progress, power- and area-efficient SAR ADCs can possibly replace pipelined ADCs in nanometer scaled CMOS processes. In this work, several circuit design techniques for SAR ADCs are proposed. According to the measurement results of the proof-of-concept prototypes, the proposed techniques are able to improve the operating speed and achieve excellent energy efficiency. The proposed techniques and chip measurement results are sketched as follows:

The first technique is a monotonic capacitor switching procedure. Compared to the conventional procedure, the average switching energy and total sampling capacitance are reduced by about 81.3% and 50%, respectively. A 10-bit, 50-MS/s SAR ADC with the proposed switching procedure is implemented in a 0.13-μm CMOS technology. The prototype ADC consumes 0.826 mW from a 1.2-V supply and achieves an ENOB of 9.18 bit. The resultant FOM is 29 fJ/conversion-step.

The second technique is a binary-scaled error compensation method. In a medium-to-high resolution case, the DAC settling issue limits the operating speed of a SAR ADC, because the capacitive DAC is not easy to stabilize in a short time interval. We insert extra binary-scaled compensation bits to compensate the DAC settling error. Accordingly, the comparator can do comparison before the DAC is well-settled, and the operating speed can be improved. A 10-bit, 100-MS/s SAR ADC using the proposed binary-scaled error compensation method is implemented in a 65 nm 1P6M CMOS technology. The prototype ADC consumes 1.13 mW from a 1.2-V supply and achieves an ENOB of 9.51 bit. The resultant FOM is 15.5 fJ/conversion-step.

The third technique is a capacitor switching method that using a variable window function to reduce the unnecessary switching in DAC network. This method saves 40~45% switching energy. Combined with the first technique, the average switching energy is reduced about 90% than the conventional one. In addition, this technique improves static and dynamic performance of SAR ADC. A 10-bit, 10-MS/s SAR ADC using this method is implemented in a 0.18-μm CMOS technology. The prototype ADC consumes 98 μW from a 1-V supply and achieves an excellent ENOB of 9.83 bit. The resultant FOM is only 11 fJ/conversion-step.