## D10-094

作品名稱

# 具可變頻率控制及適應性補償之電流模式切換式穩壓器

# A Current-Mode Switching Regulator with Variable-Frequency Control and Adaptive Compensation

隊伍名稱

**綠能切換 Green Switching**

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## 作品摘要

隨可攜式產品市場高度成長，為延長其使用電池時之待機時間，高效率電源管理晶片需求亦大幅增加。一般切換式穩壓器(switching regulator)之電源管理晶片常遭遇相當大的負載電流及輸入電壓變動，且在此變動範圍內仍需維持高效率。因此設計上會遭遇以下三個問題：其一，隨負載電流或輸入電壓不同，切換式穩壓器中各種功率損耗的絕對值及比重都會變動，難以在不同負載電流或輸入電壓下最佳化穩壓器功率效率。其二，當負載電流變化範圍大時，輕載與重載之電壓調節迴路穩定度難以同時最佳化。其三，電流控制模式需內建線性電流偵測器，此偵測器在重載時會造成可觀功率損耗。

針對上述三個問題，本作品分別提出改善方法。首先，提出可變頻率控制(variable- frequency control, VFC)方法，在不同負載電流及輸入電壓下，適應性變化切換頻率以最佳化整體功率效率。此電路不需複雜演算法，具低複雜度及低成本優點，此外還具有降低電磁輻射干擾之效果。此方法可使用於各種升降壓切換式穩壓器。對第二個問題，我們使用適應性補償器(adaptive compensator)分別針對輕重載最佳化電壓調節迴路之頻寬及相位邊限。最後，我們提出片段線性電流偵測方法，在重載時節省功率損耗且不影響輕載時電流感測精確度。

為了驗證所提出方法，本作品使用0.35um 3.3V CMOS製程設計並實現了一個積體化電流模式切換式穩壓器，晶片面積為1.05mm$^2$。量測結果顯示，切換頻率變動範圍為200kHz~2MHz，最高功率效率可達95.4%。就所知目前已發表於國際權威期刊或研討會論文之積體化切換式穩壓器都僅集中在輕載效率之改善，相較之下，本作品所提VFC可於單一晶片內同時改善輕載及重載效率。不僅如此，本作品因使用所提方法，在全負載範圍內均有改善，量測結果在輕載及重載效率分別可改善達17%及1%，所節省的功率損耗分別可達16mW及15mW。負載電流範圍為0~1050mA，與相同製程下已發表在國際權威期刊之結果相比為最大者。此外本作品所佔面積較小。因此本作品所實現電路之效能遠勝以往技術。

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- 郭教授於1988年和1990年於美國馬里蘭大學分別獲得電機工程碩士和博士學位。1992年加入成功大學電機系(所)迄今，並於2004~2007年借調集新科技及晶豪科技分別擔任總經理及副總經理。
- 專長領域：主要研究類比及混合信號積體電路設計，包含ADC、DAC、Delta-Sigma技術及class-D amplifier。近年來並致力於綠能積體電路設計，包含太陽能/風力發電之最大功率追蹤、市電併聯微型換流器、智慧型大功率馬達驅動器及變頻技術等。

## Abstract

With the rapidly growing market of portable electronic devices, high-efficiency power management ICs, which are required to extend the standby time of the portable devices powered by batteries, are in widespread demand. Switching regulators, as a kind of power management IC, often suffer from large input voltage variations. Furthermore, the regulators should be designed to maintain high efficiency in large load ranges. Therefore, three design challenges will be encountered when achieving large load ranges. First, the conduction-loss will be larger with large load current. Although increasing the size of power MOSFET can reduce the conduction-loss, the switching-loss will also be increased. Second, with large load current range, it is difficult to optimize the stability of the voltage regulation loop in both light and heavy load and the output voltage variation will also be increased. Third, conventional current sensor, which is often built-in current-mode control, is designed with fixed current scaling ratio. Therefore, the controller power-loss will be increased with larger load current.

This work presents the solutions to the above three problems. First, a variable frequency controller (VFC) circuit is proposed to adaptively selecting optimal switching frequency according to different loads and input voltages. Without complex digital circuits, the VFC can be implemented with low-cost and low-complexity circuit. The electro- magnetic interference (EMI) can also be reduced with VFC. Besides, the VFC can be applied to different converter types. Second, adaptive compensator is adopted to optimize the bandwidth and phase margin of the voltage regulation loop in both light and heavy loads, respectively. Third, a piecewise linear current sensing technique is proposed to save the power-loss in heavy load without sacrificing the sensing accuracy in light load.

An integrated current-mode DC-DC buck converter is designed and implemented with 0.35um CMOS process to illustrate the proposed techniques. The chip size is 1.05mm$^{2.}$ With 3.3V input voltage and 1.8V output voltage, the switching frequency is 200kHz ~ 2MHz and the measured efficiency can be up to 95.4%. To the best of our knowledge, all other published IEEE journal and conference papers are focused on light-load efficiency improvement. This work, with the proposed VFC technique, is the only one which can improve both light and heavy load efficiencies in the same chip concurrently. In addition, all the efficiencies in the load range are improved with the proposed VFC technique. The measurement results revealed the light and heavy load efficiencies are improved 17% and 1%, respectively. The saved power losses in light and heavy load are 16mW and 15mW, respectively. The load current range is 0~1050mA. Compared to other published papers with the same process, the load range is the largest. Besides, the chip area of this work is smaller. These results reveal that the techniques in this work are superior with other prior arts.