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作品名稱 **高速可適性接收機設計**
High-Speed Adaptive Receiver Design

隊伍名稱 **Blizzard-link**
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作品摘要

晶片A：
此晶片設計重點希望著墨在找一個新的演算法去達到可適性等化器，有別於傳統用類比控制方法，用數位方式去調整等化器的增益，且可適性數位電路不需要工作再同步的資料速率以達到高速低功率的目標。另外同樣也不需要slicer，因為不但難設計也會增加功率消耗，最後是此可適性等化器可以還原訊號即時一開始眼圖是關閉的情況下。

晶片B：
我們提出了一個新的DFE的架構，叫做adaptive DFE-IIR，我們取代了傳統multi-feedback DFE，我們只使用一路無限脈衝回授(IIR feedback)就能達到multi-taps ISI的補償。無限脈衝響應濾波器的實現方式是使用一階的RC filter。在這邊我們必須要適當的去調整RC time constant還有amplitude，使得IIR Filter的輸出端可以完全的跟接受訊號的ISI消除。

ABSTRACT

Chip A: A 20Gb/s Digitally Adaptive Equalizer/ DFE with Blind Sampling.

As data rates increase, the backplane communication systems suffer from serious inter-symbol interference (ISI). Due to different channel lengths, loss, and environment variations, an adaptive equalizer is an attractive and robust circuit to equalize the received data in high-speed data communications. Several techniques are presented for adaptive equalizers. A spectrum balancing method is presented for an analog equalizer. However, this method is valid only for the random data with fixed data rate. An eye-opening-monitor (EOM) method adopts a two-dimensional map to detect the signal quality. This EOM method needs a synchronous sampling clock and high-speed comparators. It results in high power consumption and furthermore it requires accurate analog circuits.

Chip B: A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization.

Conventionally, a multiple-tap DFE is adopted to compensate the inter-symbol interference (ISI), which is induced by postcursors due to the non-ideal channel impulse responses. To avoid the power and area penalty due to many postcursors, a DFE with infinite impulse response (MR) filter feedback has been presented. In [B. Kim et al., 2009], no adaptation scheme ensures that such MR filter cancels the postcursors precisely, i.e., its RC time constant and amplitude need to be manually adjusted. In this work, a 6Gb/s receiver using a DFE with an adaptive continuous-time MR filter and a clock/data recovery (CDR) circuit is presented. In a high loss environment, a conventional digital qaudricor relator frequency detector (QFD) may fail due to the significant data dependent jitter. To integrate an adaptive DFE with a CDR circuit, a proposed frequency sweeping frequency detector (FD) and a lock detector (LD) are presented in this work.