Design Group

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作品名稱 **適用於電流引導式數位類比轉換器之無雜散動態範圍提升技術**

SFDR Enhancement Technique for Current-Steering Digital-to-Analog Converter

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作品摘要

因應高速操作，電流引導式架構是被廣泛採用的，然而，非理想的電流切換限制了無雜散動態範圍的頻寬，當輸入之數位信號達高頻時無雜散動態範圍也急速下降。為了保持良好的高頻無雜散動態範圍，本作品提出「數位式亂數歸零法」，且吾人實現一個八位元、每秒十六億個取樣之數位類比轉換器此數位類，其無雜散動態範圍優於六十分貝，直至輸入頻頻高達四點六億赫茲，功率消耗量為九十毫瓦。

當高解析度的電流引導式數位類比轉換器是必須時，電流源就得高度滿足匹配特性，其付出的代價
即為大面積且本質電容、雜散電容也變大因而導致頻寬下降，改善此現象的途徑為使用較小面積的電流源。然而，小面積電流源將引起嚴重的不匹配，本文提出一個背景校正技術來保確高精準度。

為驗証此背景校正理論，吾人實現一個十二位元轉換器。此轉換器功率消耗為一百二十八毫瓦，操作速度可達每秒十二點五億個取樣。當頻率高達五億赫茲時，此數位類比轉換器有優於七十分貝之無雜散動態範圍。

ABSTRACT

This work focuses on the Digital-to-Analog Converters (DACs). The current-steering structure has been widely used in high-speed DACs, since in this structure the main speed limitation comes from the output node, and high sampling speed is thus easily achieved. However, the non-ideal switching limits the bandwidth of spurious-free dynamic range(SFDR). The SFDR decreases rapidly with increasing input frequency. Therefore, Digital Random Return-to-Zero(DRRZ) is proposed for the high sampling rate current-steering DAC to maintain high SFDR at high frequency.

To demonstrate the proposed Digital Random Return-to-Zero technique, a CMOS 8-bit 1.6-GS/s DAC was fabricated in a 90 nm CMOS technology. The DAC achieves a SFDR better than 60 dB for a sinewave input up to 460 MHz, and better than 55 dB up to 800 MHz. The DAC consumes 90 mW of power.

In the design of high-accuracy current-steering DACs, current sources with high matching property are required and the penalty is large area. Intrinsic and parasitic capacitor loading also degrade the signal bandwidth. The way to reduce loading is using compact current cells. In this thesis, background calibration is proposed to correct the mismatch current caused by small dimension.

To verify the proposed background calibration algorithm, a 12-bit DAC was fabricated in 90nm CMOS technology and using compact current cells. The area of current sources are 1/400 of the required area which is designed for 12-bit resolution. The chip consumes 128mW. Active area is 1100umx750um. At 1.25GS/s sampling rate, the DAC achieves better SFDR than 70dB up to 500MHz input frequency.