Design Group D11-066

作品名稱

應用於GNSS之全積體化雙頻離散時間接收機
Fully-Integrated Dual-Band Discrete-Time Receiver for GNSS Application

隊伍名稱
九地 Anywhere

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作品摘要

創作動機

聯合國(COPUOS，Committee on the Peaceful Uses of Outer Space)於2001年開始主導Global Navigation Satellite System(GNSS)，其中包含許多國家自行研發的系統：美國的GPS，俄國的GLONASS，歐盟的Galileo，以及近幾年有顯著發展的中國的Compass/Beidou（北斗），將針對不同功能需求提供全世界全球定位服務。

因此，如何(1)從設計觀點中，有效地利用各個系統的優點；(2)在工程上，適應製程的演進(process immigration)；(3)面對大環境，能夠響應綠能概念(green power)。若能結合以上幾項的特色，我們可以提供一個完整、實際和極具吸引力的解決方案！

系統簡介

本作品的目標鎖定在GNSS中的GPS以及Galileo，皆屬於CDMA(Code-Division Multiple Access)；本接收機可以接收其中的L1(1.57542 GHz)以及L5(1.17645 GHz)頻段的訊號，總共有十一種訊號。由於功能的需求不同，擁有不同訊號的頻寬，分別是4.092 MHz(L1)以及10.23 MHz(L5)。考量到GNSS的訊號相較於一般通訊系統的訊號要來的微弱(-168 dBm)，對於flicker noise(corner frequency ~ 1 MHz)的影響更加嚴重，進而造成sensitivity降低；架構上採用low-IF(Intermediate Frequency)來避開它。在射頻電路的部分，低雜訊放大器(LNA)可以控制欲接收的頻段，之後由image-rejecting mixer將RF訊號下降至所需要IF的位置；在類比頻段的部分，我們採用了離散時間濾波技術(discrete-time filtering technique)，藉由數位電路控制可程式化的電容陣列，實現了可調整頻寬的濾波器。系統化接收機的可程式特性可以搭配DSP(Discrete-time Signal Processing)的需求做切換，即使在失去對特定系統衛星的追蹤時，可以迅速轉換接收另外一個系統的訊號。讓整體效能提升！

實作結果

我們採用了0.18-μm 1P6M CMOS製程設計與實現了一顆全積體化的接收機：從射頻的LNA，image-rejecting mixer，以及產生特定頻率的頻率合成器，到類比頻段調整接收頻寬的離散時間濾波器。尤其在濾波器方面：(1)藉由數位控制，過濾出頻寬4.092 MHz以及10.23 MHz的訊號；(2)優異的抗製程變異特性，讓模擬和實作之間的差異可以減小；(3)較少使用類比元件的天性，使得我們的接收機可以隨著製程演進可以降低成本；(4)利用數位操作的獨特性，在靜態上不耗電！

指導教授

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- Professor Yi-Jan Emery Chen received the B.S. degree in electrical engineering from National Taiwan University, Taipei, Taiwan, R.O.C., in 1987, the M.S. degree in electrical and computer engineering from the University of California at Santa Barbara, CA, in 1991, and the Ph.D. degree in electrical engineering from the Georgia Institute of Technology, Atlanta, in 2001.
- Since 2003, he has been with National Taiwan University, Taipei, Taiwan, R.O.C., where he is currently an Associate Professor. He has authored or coauthored over 70 refereed journal and conference papers.
- Research focus: the design of RFIC, RF power amplifier, LCD driver / LED driver IC, power management IC, LTPS IC, and System-in-Package integration.

ABSTRACT

Motivation

For providing the global-positioning services in different applications, in 2001, the COPUOS (Committee on the Peaceful Uses of Outer Space) started to hold the development on Global Navigation Satellite System (GNSS), which is almost based on nation's development including US' GPS, EU's Galileo, Russia's GLONASS, China's BeiDou/Compass, and other regions systems.

Therefore, how to (1) utilize the pros of each system in viewpoint of design; (2) be suitable with process immigration in viewpoint of manufacturing; and (3) follow the green-power trend for our Earth. If the above points can be achieved, we can provide a complete, practical, and attractive solution!

Idea

Our target focuses on the L1 (1575.42 MHz) and L5 (1176.45 MHz) bands in GNSS, which are all CDMA (Code-Division Multiple Access) systems; totally 11 different signals can be captured by our receiver. Because of different applications, the signal bandwidth is different; they are 4.092 (L1) and 20.46 (L5) MHz. While the GNSS signals are relatively weak (-168 dBm) comparing to other communication systems, the flicker noise (corner frequency ~ 1 MHz) may has a big impact on the signals and then degrade the sensitivity; thus, our receiver architecture is low-IF (Inter-mediate Frequency) which can avoid the low-frequency noise after down-conversion. In RF (Radio Frequency) part of the receiver, the LNA (Low-Noise Amplifier) can select wanted band and the image-reject mixer will down-converts the RF signal to required IF location. In analog part, we use the discrete-time filtering technique to design and implement a bandwidth-programmable filter by digitally controlling a programmable capacitor array. The programmability of the systematic receiver can be integrated and controlled by the DSP (Digital-Signal Processing); when we lose the tracking to the arbitrary satellites, the receiver can rapidly switch and re-track the signals which are more environmentally resistive. Therefore, the overall performance can be enhanced!

In addition to the programmability, the discrete-time (D.T.) receiver uses less analog components (i.e. resistor), and applies many MOS switches and capacitors. Because the analog components are easy to vary with the P.V.T. (Process, Voltage, and Temperature), traditional analog filters need trimming after the chips are back from foundry. In our design, the discrete-time filter has a characteristic, which depends on the ratio value, and the ratio can be precisely controlled in modern CMOS process! Further, the D.T. filter is under digital control, so it has no static power consumption! Besides, in the viewpoint of process, the MOS device and capacitor will become smaller as the process immigrates. The D.T. filter, which utilizes the switches and capacitor array, will also be smaller in area, following process immigration! Just like digital circuits! We can predict that the cost will be decreased!

Results

We use 0.18-μm 1P6M CMOS process to design and implement a fully-integrated receiver, which contains switchable LNA and image-reject mixer at RF, a frequency synthesizer, and bandwidth-programmable D.T. filter. Especially in D.T. filter, (1) we can filter out 4.092-MHz and 10.23-MHz signals by digital control; (2) excellent process tolerance keeps the difference between simulation and implementation small; (3) with less analog components, our design can follow the process immigration, so the cost will be decreased; (4) due to digital control, no static power consumption!