# D13-018

## *Yield and Reliability Enhancement Techniques for Emerging Memory Technologies*

## 先進記憶體之良率與可靠度改善技術

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## 作品摘要 Abstract

本企劃主要提出改善 NROM 等相關非揮發性記憶體良率與可靠度之相關技術。NROM 具有高資料儲存能力、低製造成本以及較好的數值穩定性。它也有望取代以浮動閘（Floating gate）為基礎的非揮發性記憶體。

為了提升製程的良率以及改善可靠度，我們提出了一種新的測試與修復流程如圖一所示。在製程上發生的錯誤，當顧客所提供的資料寫入後，考量到其在邏輯上顯現的故障效應，提出了錯誤遮蔽（Fault masking）技術。我們提出了具有高遮蔽可能性的錯誤遮蔽技術—位址不規則性（Address scrambling）技術，同時也建立針對此遮蔽技術的圖學模型，另外 Address Scrambling 可包括 Row Scrambling 與 Column Scrambling，並能進一步將兩者整合為 Hybrid Scrambling 技術。所提出的方法也很容易整合於現有的內建自我測試電路中。本企劃書也提出 Code Scrambling 的技術，其目的同樣在於增加錯誤遮蔽的機會，只要能將許多不同的顧客程式碼寫入適當的 NROM 裡，就能增加錯誤遮蔽的機會，而從實驗數據中可以發現，我們所提出的方法都能使製程良率大幅提升。我們也開發故障模擬器以進行修復率（Repair rate）的分析。

NROM is one of the emerging non-volatile-memory technologies, which provides very high data density, low fabrication cost, and better value stability. It is also promising for replacing current floating-gate-based non-volatile memory such as flash memory.

In order to raise the fabrication yield and reliability, a novel test and repair flow is proposed in this project. Instead of the traditional fault replacement techniques, fault masking techniques are also exploited by considering the logical effects of physical defects when the customer’s code is to be programmed. Two techniques are also proposed to maximize the possibilities of fault masking—address scrambling (include row scrambling and column scrambling) and code scrambling. Moreover, the row and column scrambling techniques can be merged as the hybrid scrambling technique. Graph models are also presented for modeling these methods. The proposed methods can be easily incorporated into the ROM BIST architectures. According to experimental results, the fabrication yield can be improved significantly. Moreover, the incurred hardware overhead is almost negligible.

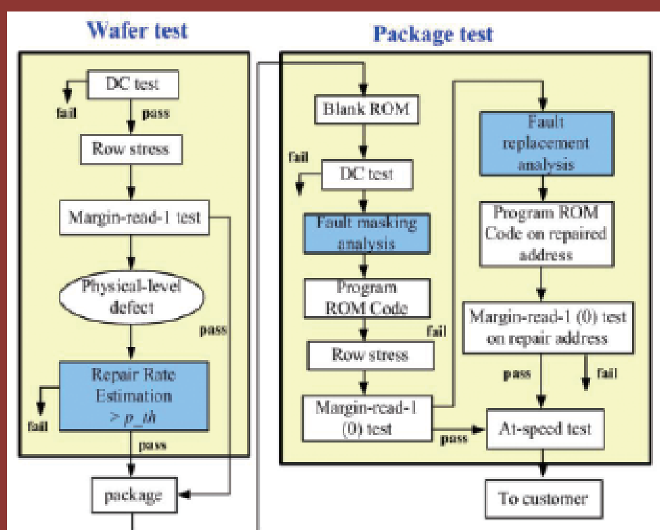


圖1 > NROM新的測試與修復流程