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A 60-GHz Fully Integrated CMOS Sub-Harmonic RF Transceiver Front-End with Integrated Artificial-Magnetic-Conductor (AMC) On-Chip Yagi-Antenna and Balun Bandpass-Filter For Very-Short- Range (VSR) Gigabit Communications

應用於極短距離 Gigabit 無線通訊的 60-GHz 整合 CMOS 人造磁導體 Yagi 天線及平衡式濾波器之毫米波次諧波射頻前端收發機晶片

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作品摘要

本研究使用CMOS 90-nm製程，研製一個『整合毫米波CMOS on-chip人造磁導體（artificial-magnetic-conductor，AMC）天線及平衡轉非平衡式帶通濾波器之60-GHz CMOS次諧波射頻前端收發機』毫米波射頻晶片，此毫米波晶片包含AMC結構之Yagi天線、平衡轉非平衡式帶通濾波器（balun-BPF）、高隔離度收發開關（T/R switch）、功率放大器（PA）、低雜訊放大器（LNA）及主動式次諧波降頻混頻器（SHM）。天線主體選用高指向性Yagi天線，其高指向輻射場形之特性適用於CMOS射頻晶片嵌入式天線設計。此外利用AMC結構在共振頻率時，形成高阻抗表面的特性，使天線產生建設性干涉的功效，能有效增加輻射效率與輻射增益。濾波器結合零度與非零度饋入技術形成具有180度相位差的平衡轉非平衡式帶通濾波器，以減少額外元件損耗及晶片使用面積。收發開關以串並式架構實現，並利用相位差180度的兩相似路徑使發射端洩漏訊號可以被消除，進而提升收發端之間的隔離度。功率放大器採用A類之偏壓形式來達成較佳之線性度，並採用三級串接達到高功率增益，以減輕前級電路的設計負擔。低雜訊放大器採疊接組態做為電路核心，在前兩級電路間加入電感以達雜訊匹配最佳化，有效抑制雜訊。主動式次諧波混頻器採適用於低電壓操作的單平衡式串接形態之LO架構，利用非線性效應於開關電晶體汲極端產生二倍頻訊號後與RF訊號混頻，此舉能降低振盪器的設計負擔並適合設計於毫米波頻段。此CMOS射頻前端收發機整合晶片之發射端整體發射增益為5dB，發射訊號強度約為-18.4dBm；接收端整體接收轉換增益為10.1dB。此晶片亦完成了16QAM-OFDM之數位調變量測。本研製之毫米波射頻收發晶片對極短距離（very short range，VSR）Gigabit無線通訊之應用將有助於提供一高整合性、低成本之收發機單晶片設計方案。

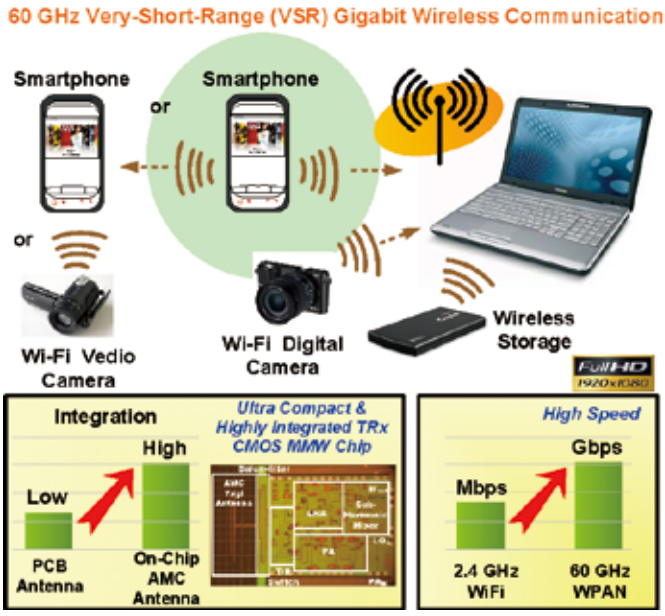

圖1 > 應用於60 GHz極短距離Gigabit之點對點、高速率無線傳輸應用情景

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分別於 1977、1981 年取得臺灣大學學士、碩士學位，並於 1987 年獲得美國密西根州立大學電機博士學位，同時於該大學工學院研究中心任博士後研究員，1988-1990 年為美國摩托羅拉公司無線電部門研究工程師。目前為成功大學電機工程系 / 電腦與通信工程研究所教授。

研究領域

射頻微波 / 毫米波無線通訊積體電路 / RF-SoC、無線通訊天線與被動元件、微波 / 毫米波通訊與感測 sensor 系統、電磁數值計算及生物電磁之醫學工程應用、電磁輻射 / 干擾（EMI/EMC）計算測量。

Abstract

A 60-GHz millimeter-wave (mm-wave) CMOS sub-harmonic RF transceiver with an integrated on-chip artificial-magnetic-conductor (AMC) Yagi-antenna and a balun-bandpass-filter (balun-BPF) fabricated in 90-nm technology is presented. As shown in fig. 1, the proposed mm-wave RF transceiver consists of an on-chip AMC Yagi-antenna, a balun-BPF, a high isolation T/R switch, a power amplifier (PA), a low-noise amplifier (LNA) and a single-balanced down-conversion sub-harmonic mixer (SHM) combined with an active balun. The Yagi-antenna with a high directivity pattern is adopted in on-chip antenna design. The AMC structure on the CMOS bottom metal (M1) can act as a perfect magnetic conductor (PMC) when resonant to render a high impedance surface. The high impedance surface can reduce the EM field induced in the lossy substrate and improve the loss (which will increase the antenna efficiency from 5 to 15%). Also, the constructive interference is occurred due to the PMC boundary condition of AMC at resonant frequency. From these two characters of the AMC structure, the CMOS on-chip Yagi-antenna power gain can then be increased from -12.5 to -7.5 dBi. The CMOS 180° -phase difference balun-BPF integrates the design of balun and RF BPF to reduce the chip size and the insertion loss. A simplified single-pole double-throw (SPDT) T/R switch with the leakage cancellation technique is used to increase the isolation between the Tx and Rx ports. The leakage cancellation technology with two transistors and two 90-degree phase shifters is used in this switch design in which the leakage signal is reduced by propagating through two similar paths with 180° phase difference. The class-A PA is utilized to achieve high linearity and power gain. The three-stage cascode configuration is adopted to maximize the power gain in order to relieve the burden of pre-stage circuit. In LNA design, a 2-stage cascode structure with a common-source (CS) buffer amplifier is adopted. A microstrip line inductor is inserted in each cascode structure for noise reduction. A bottom-LO single-balanced down-conversion SHM with an active balun is adopted to down-convert the receiving signal. It can operate at low supply voltage and thus reduce the power consumption. Since the $2f_{LO}$ signal can be obtained at the common-drain node of the switching pair by utilizing nonlinear effect, the design complexity of the oscillator can be reduced. Two Marchand baluns are integrated into the mixer at the RF and LO input nodes to provide differential signals. The active balun combines the differential output IF signal buffered by a CS amplifier. The probe-station based on-wafer continuous wave (CW) wireless transmission test is conducted (R = 1 m). The measured total transmitting gain G_{ant+Tx} and receiving conversion gain CG_{ant+Rx} of the integrated RF transceiver are about 5 dB and 10.1 dB at 60.1 GHz, respectively. The effective isotropic radiation power (EIRP) of the integrated transceiver (with on-chip antenna) is about -18.4 dBm under the PA input power of -23 dBm. In the digital-modulation transmission test, the maximum data rate of the RF transceiver in 16QAM mode at a 50-cm wireless link has been investigated from error vector magnitude (EVM) measurement. The presented integrated mm-wave RF transceiver will be very useful for the design of a 60 GHz fully integrated CMOS single-chip radio for very-short-range (VSR) wireless gigabit communication applications.

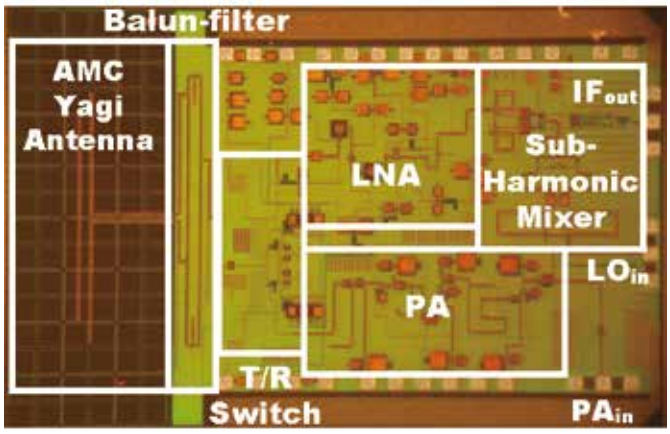

Fig.2 > A 60-GHz fully integrated MM-wave CMOS sub-harmonic RF transceiver front-end with integrated artificial-magnetic-conductor (AMC) on-chip Yagi-antenna and balun bandpass-filter (chip size= 1.5 × 2.34 mm2)