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Fault Scrambling Techniques for Reliability and Yield Enhancement of Non-Volatile Memory

以故障分散技術提升揮發性記憶體的可靠度與良率

隊伍名稱
可靠隊 / Reliability of STARs

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作品摘要 Abstract

近幾年，快速發展的超大型積體電路技術造成了電晶體的尺寸明顯減小、記憶體細胞的密度也急速增加，在2014年時，嵌入式記憶體將會占系統晶片設計面積高達94%，由此可知，記憶體主導了整顆晶片的良率和可靠度，而記憶體修復或是容錯能力變得相當重要。為了解決這種困境，本企劃提供了一種新的測試與修復流程如圖一，並提出一個有效的故障分散技術（Fault Scrambling Technique），有別於傳統的故障偵測與更正技術，我們嘗試更改編碼字之組成記憶體細胞，使得每個編碼字中故障細胞的數目均在其更正能力之內。

本企劃也提出相對應的雜散電路（Scrambling Circuits）與自我分析電路（Built-In Scrambling Analysis，BISA）如圖二，利用內建自我測試（Built-In Self-Test，BIST）電路提供可靠的故障細胞資料，經過BISA計算出有效的雜散控制字（Scrambling Control Word），最後送進雜散電路，控制雜散電路是否對相對應的位址位元（Address Bit）做出反轉的動作，藉此我們可以把原本的實體位址（Physical Address）轉換至新的邏輯位址（Logical Address），而後再進入解碼器進行記憶體存取，讓存入的資料將會以雜散過後的的位址寫入記憶體陣列之中，進而讓故障細胞分散到不同的1編碼字，以達到一個編碼字中的記憶體細胞最多只含有一個故障細胞，使更正碼可修正故障細胞，提升良率和可靠度。

With the ever-increasing VLSI technologies, the miniaturization of transistors makes embedded memories smaller and denser. It then inevitable affects the reliability and yield of the manufactured products. Moreover, according to the Semiconductor Industry Association (SIA) and ITRS reports, embedded memories will occupy up to 94% relative silicon area of a system chip by 2014. Therefore, embedded memories will dominate the yield of system chips. We proposed a new test and repair flow with the fault scrambling techniques integrated as shown in Fig. 1.

Instead of merely using redundant rows/columns to replace faulty cells, error-correcting codes are also considered an effective technique to cure permanent faults for the enhancement of fabrication yield and reliability of memories. However, the protection capability of the widely used SEC-DED (single-error correction and double-error detection) codes will be limited if a codeword contains multiple faulty bits. In order to cure this dilemma, efficient fault scrambling techniques are proposed. Unlike the fixed constituting memory cells of a codeword in the conventional EDAC schemes, we try to refigure the constituent memory cells of codewords such that each codeword consists of at most one faulty cell. The BISR architecture which can perform the fault scrambling technique is shown in Fig. 2. It mainly consists of the BIST module, the RAS (Row Address Scrambler), the CAS (Column Address Scrambler), and the built-in scrambling analysis (BISA) module. According to experimental results, the repair rates can be improved significantly with negligible hardware overhead.

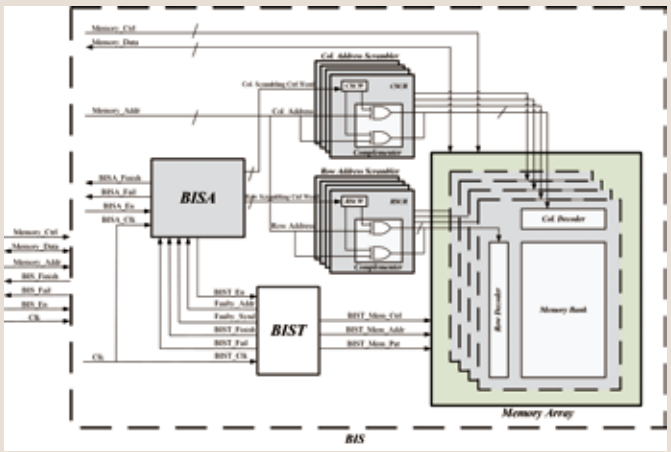

圖1 > 基於錯誤分散技術並加入BISA之BISR架構圖

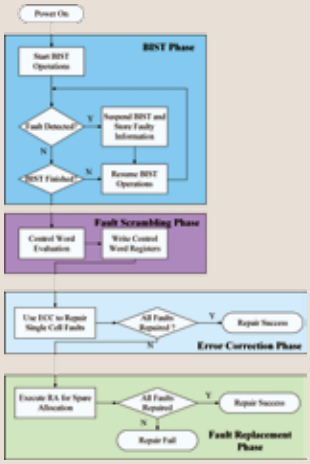

Fig.2 > The proposed test and repair flow with the fault scrambling techniques incorporated