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25Gbps Equalizer and Clock and Data Recovery Circuit

25Gbps 等化器與時脈資料回復電路

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作品摘要 Abstract

隨著科技的進步，每人每天使用的資訊量爆炸性成長，為了即時處理這些龐大的資料，硬體的規格要求也越來越高。在有線傳輸系統中，發送晶片 (Transmitter, TX) 與接收晶片 (Receiver, RX) 之間必須經由印刷電路板 (Printed circuit board, PCB) 上的通道交換訊號，然而在越快的傳輸速度下，資料經過通道後的衰減將越嚴重。假設欲傳輸的資料速度為 25 Gbps，其尼奎斯特頻率 (Nyquist Frequency) (12.5 GHz) 上的資料通道衰減約為 20dB。當印刷電路板上的傳輸線長度越長，衰減量也會更加嚴重，雖可使用新的傳輸材料來得到較佳的通道響應，但成本也會跟著增加。

本團隊提出一個操作在 25Gbps 的接收器，由連續時間線性等化器與內建 2-tap 決策回授等化器的時脈資料回復電路組成。操作在 19Gbps 到 25Gbps 的範圍中，混合式的半速率時脈資料回復電路能幫助消除符際干擾與資料抖動。並提出一個不需使用電感並提供取樣時脈相位的四相位弛張震盪器。此晶片使用台積電 40 奈米互補式金氧半導體製程，全部接收器消耗 84.5 毫瓦，操作在 1.2 伏特電壓，晶片核心電路面積為 0.09 平方毫米。

With the advancement of technology, the amount of daily information used by each person is growing explosively. In order to deal with this huge instant information, the hardware specifications are also increasing. In cable transmission systems, transmitter(TX) and receiver(RX) must communicate through the channel on the printed circuit board(PCB). However, the faster the transmission speed, the more severe loss of data transmission through the channel. Suppose we want to transmit the data at speed of 25Gbps, the data loss at the Nyquist Frequency(12.5GHz) is about 20dB. In addition, increasing the transmission channel length of the PCB will increase the data loss. Although we can use the new materials to get a better channel response, the cost also increases.

This paper describes a 25-Gb/s receiver comprising of a continuous time linear equalizer followed by a 2 tap decision feedback equalizer. The hybrid half-rate CDR facilitates ISI and jitter suppression over 19 Gbps-25Gbps operation. A quadrature relaxation oscillator provides the sampling phases without bulky inductors. Fabricated in a 40 nm CMOS technology, the whole receiver consumes 84.5mW from 1.2 V supply with a core area of 0.09 mm².

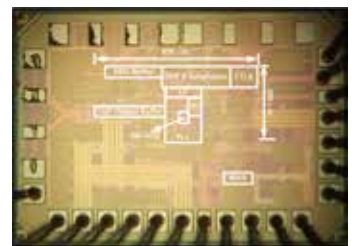


Fig.2 > Chip photo.

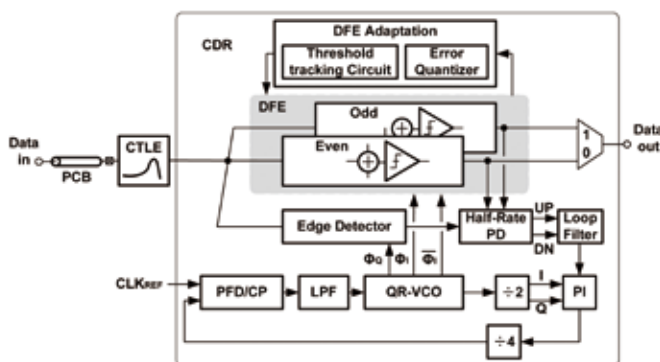


圖1 > 接收機架構圖

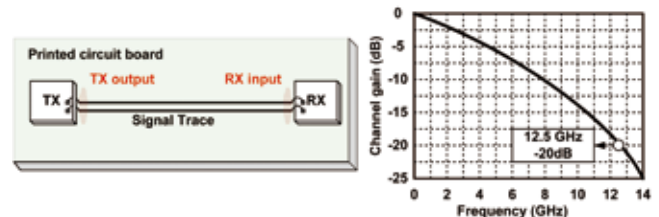


Fig.3 > Cable transmission system and channel frequency response.