D15-069

A Single-Channel 10-bit 160-MS/s Successive-Approximation Analog-to-Digital Converter with Compact Architecture and Noise Suppression Techniques in 90nm CMOS

一個精簡架構且具雜訊壓抑技巧的使用 90 奈米製程的單通道 十位元每秒取樣一億六千萬次的逐漸趨近式類比數位轉換器

隊名 高速「SAR」不住 ADC
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作品摘要

在過去幾年，智慧型手機、高性能數位電視和無線區域網等電子產品蓬勃發展，在這應用中需要一個幾十到幾百取樣頻率（MS/s）、中高解析度（8~12 bit）的類比至數位轉換器（ADC），這樣規格的數位至類比轉換器長期由管線式（pipelined）架構所主宰。然而，逐漸趨近式類比至數位轉換器（SAR ADC）相對於其他架構而言，隨著製程的演進，其操作速度越來越快且面積越來越小。在先進製程中，SAR ADC 已漸漸可以取代部分管線式類比至數位轉換器所主宰的取樣範圍。因此，我們這次的作品，將呈現了一系列 SAR ADC 的設計與實作介紹，透過實際的晶片下線和量測驗證，證實所提出之電路設計技術可以有效提升電路的操作速度以及降低每次轉換所消耗的能量。

此作品提出三種新技巧更進一步提升逐漸趨近式類比至數位轉換器的電路性能，第一個技術為精簡組合電路時序控制，其簡化數位控制電路，節省其動態功率消耗，並去除傳統架構中浮動節點的漏電問題，降低漏電的功率消耗並使電路更加穩固。第二，我們提出非同步電路時脈改善技術，藉由同時將比較器輸出端電位的變化情況與電容陣列的上板電壓的穩定情形納入考量，依此來最小化數位電路的延遲時間，提升逐漸趨近式類比至數位轉換器的操作速度。第三，我們提出雜訊壓抑技術，在不消耗更多比較器功率的前提下，提升比較器的精確度。整體架構圖如圖一所示。

本設計使用台積電 90-nm UTM CMOS 製程來實作晶片，圖二為整個晶片的照相圖，整體晶片大小為 0.8836mm2，其長寬為 940 μm × 940 μm，其中核心的面積為 0.01396mm2，其長寬為 178.4 μm × 78.25 μm。從實際晶片量測結果顯示，此晶片在 1 伏特的電壓與每秒取樣一億六千萬次取樣的操作速度下，總消耗功率為 1.12 mW，有效位元數為 9.03 bit，每次資料轉換所消耗的能量為 13.4fJ，DNL 與 INL 分別為 +0.3/-0.69 LSB 與 +0.59/-0.55 LSB。圖三是近年來發表在國際期刊 ISSCC 或 Symp. VLSI circuit 中能源轉換效率與取樣頻率的規格性能，從圖中可以看出此作品的規格性能儘管是用較不先進的製程，和先進製程比起來，仍是可以在相同操作速度下，維持面積小，整體性能表現優異。

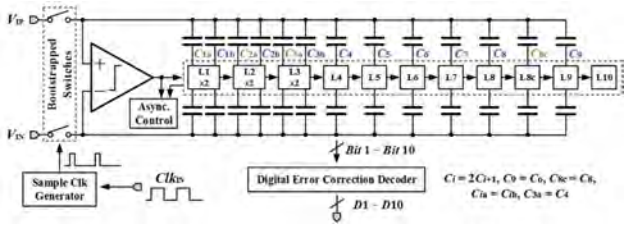

圖 1 / 此晶片整體 SAR ADC 架構圖

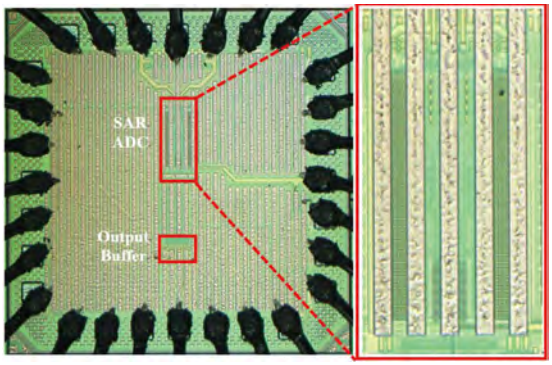

圖 2 / 晶片及局部放大照相圖

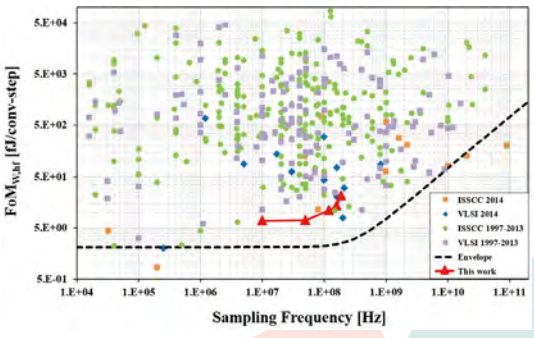

圖 3 / 能源轉換效率與取樣頻率的規格性能圖

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交通大學電機博士。2002 年任職於工研院系統晶片中心。2003 年開始進入成功大學電機工程學系擔任助理教授，2010 年獲得 IEEE Tainan Section 2010 Best GOLD Member Award，2011 年升為電機工程學系教授，並於同年擔任成功大學電機工廠主任一職至 2014 年。

研究領域

混合信號積體電路設計、測試與可測試設計、電腦輔助積體電路設計。

Abstract

In the last few years, there have been explosive growth in the electronic devices such as smart phones, high quality digital TV applications and WLAN systems. Analog-to-digital converter (ADC) with the specifications of 8 to 12 bits resolution and several tens to hundreds of MS/s is needed for driving the high data rate applications where pipelined ADC is extensively used. However, in successive-approximation register (SAR) architectures, the conversion time and power dissipation become smaller with the advancement of CMOS technologies. SAR ADC can possibly replace pipelined ADC in nanometer scaled CMOS processes. In this work, several circuit design techniques for SAR ADC are proposed. According to the measurement results of the proof-of-concept prototypes, the proposed techniques are able to improve the operating speed and achieve excellent energy efficiency.

This work proposes three techniques to further enhance the performance on SAR ADCs. First, the compact combinational timing control technique is proposed to simply digital control circuitry and to reduce dynamic switching power consumption. The leakage problem from floating nodes is also removed to lower leakage power consumption and it makes the circuit more robust. Second, the enhanced asynchronous timing scheme is proposed to minimize the digital loop delay by taking both output condition of the comparator and the DAC settling issue into consideration, so that it can promote the operating speed of the SAR ADC. Third, the noise suppression technique is proposed to reduce the input-referred noise of the comparator without increasing the power consumption. The architecture of the proposed SAR ADC is shown in Fig. 1.

The proposed SAR ADC was fabricated in TSMC 90-nm CMOS technology. The micrograph and the zoom-in view of this work are shown in Fig. 2. The chip area is 0.8836 mm2 in size of 940 μm × 940 μm, and the core area is 0.01396 mm2 in size of 178.4 μm × 78.25 μm. At 1-V supply voltage and 160-MS/s sampling rate, the power consumption of the ADC is 1.12 mW with a peak ENOB of 9.03 bit. It achieves a figure of merit (FoM) of 13.4 fJ/conversion-step. The measured DNL and INL are +0.3/-0.69 LSB and +0.59/-0.55 LSB, respectively. Fig. 3 shows the performance chart of FoM versus sampling frequency compared with the state-of-the-art of ISSCC and SoVC from 1997 to 2014. Although the prototype was fabricated by an older technology, it still achieves similar sampling frequency, small active area, and excellent FoM performance compared with those excellent works in advanced process.

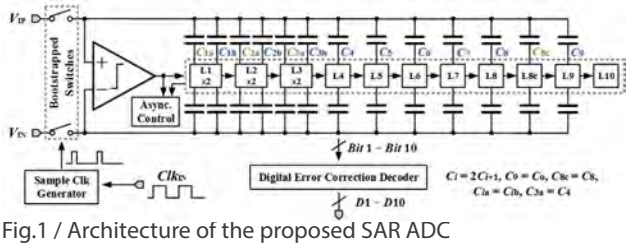

Fig.1 / Architecture of the proposed SAR ADC

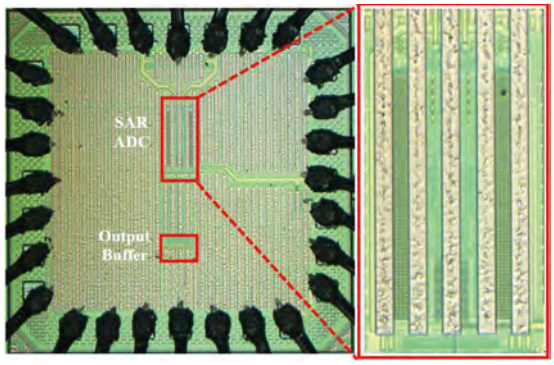

Fig.2 / Micrograph and zoom-in view of the proposed SAR ADC

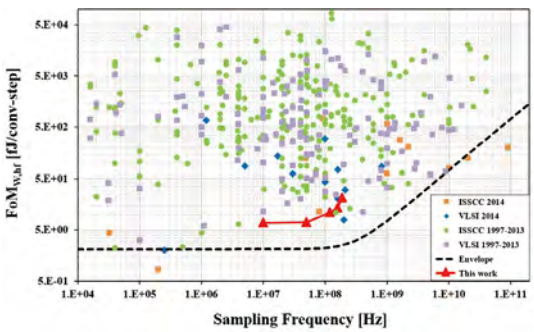

Fig.3 / Performance chart for FoM versus sampling frequency