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A 20 Gb/s SC/OFDM Dual-Mode Baseband Receiver for 60 GHz Band

應用於 60GHz 頻帶無線傳輸 20 Gb/s 的單載波 / 正交分頻多工傳輸雙模數位基頻接收器

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作品摘要

看著家中日益增多的螢幕、顯示器，是不是常常為了傳輸拉線時的美觀與空間的安排傷過一番腦筋呢？現今隨著採用 60GHz 為傳輸頻帶，我們得以使用更大的頻寬和更高的傳輸速率，達到無線傳輸的目標，而在如此高的頻帶中傳輸也伴隨著許多問題。依照電機電子工程師學會（IEEE）在 60GHz 頻帶上制訂的 IEEE 802.15.3c 和 IEEE 802.11ad 兩套國際規範，將會提供在 10 公尺的距離之內至少 1 Gb/s 以上的傳輸速率，且此兩國際規範皆有定義單一載波模式（Single Carrier，SC）和正交分頻多工模式（Orthogonal Frequency Division Multiplexing，OFDM）作為傳輸的技術。而本計畫設計的基頻接收器，將會以上面兩個國際規範中，最大的誤差容忍量為設計基準，使用 Cell-Based Design Implementation 設計，將 60GHz 中的傳輸效應消除，使錯誤率降到最低，達到高正確性的無線傳輸、並且克服相容性問題，以一套硬體達成兩套國際規範、兩種傳輸技術，一共四種傳輸方式的傳輸。並且用管線（Pipeline）與平行化技術，加高工作頻率與平行處理量，最後達到 24Gb/s 相當於 HDMI 規格所定 10.2 Gb/s 之傳輸量之 2 倍量。

而於本設計中的頻域等化器中提出一個新的概念（Window-based Noise Cancellation，WNC），可以用以消除通道估計時雜訊造成的偏差，與沒有 WNC 之通道估計相比，WNC 雜訊消除後的 MSE 整整改善了 33.58dB。而硬體上更擁有邏輯閘數低、消耗功率低等好處，除此之外，還達到了許多設計皆無法支援的 64QAM 調變方式，從單位時間的整體傳輸率來看，本設計的傳輸率將遠大於其餘等化器設計數倍之多。

Cell-Based Design Implementation 流程包含幾個主要的實現步　驟：RTL coding、Logic synthesis、Place & Route、Layout Merge，在這些實現步驟當中還穿插各種不同的驗證，驗證的目的是確保各個實現階段結果的正確性，項目包括有 function、timing、power、DRC 等，越到實體階段所須驗證的項目就越多。由於此通訊基頻接收器包含了許多關鍵模組，對於如何要整合每個關鍵模組以及整合完之後如何使用不同用途的工具來確保各個實現階段的正確性為一個相當大的挑戰。我們使用 CIC 提供的軟體，對於每個 Cell-Based Design Flow，無不仔細且謹慎的實作，以求得到最好的結果。

我們將國際規範給定的 2.64GS/s 要求提升至更高的 3.33GS/s 取樣率，根據原本企劃目標，八倍平行架構下操作頻率為 417MHz，再使用 64QAM 可達到 20Gb/s 吞吐率。關於實際的量測結果，在 Core VDD 為 0.9 V 不加壓的情況下晶片可以達到 417 MHz 的操作頻率，也就滿足本企畫吞吐率為 20Gb/s 的目標，同時消耗的功率僅需要 496.39mW。當 Core VDD 加壓 4.4% 至 0.94 V 的情況下晶片可以達到 500 MHz 的操作頻率，吞吐率可以達到 24 Gb/s，消耗功率為 697.8mW。

此結果顯示本計畫之設計成果確實可運用在室內短距離的高畫質多媒體上，而未來甚至可以展望於藉由如此高傳輸量將傳輸孔去除，進而增加機體美觀度與耐用性，使得家庭環境更加便利整潔等目標。

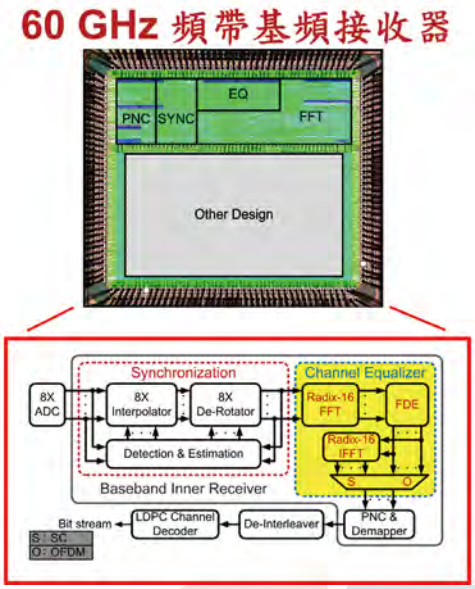
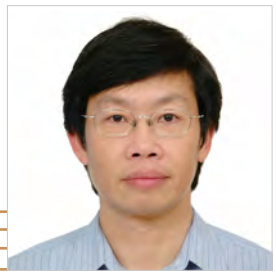


圖 1 / 60GHz 頻帶基頻接收器電路架構與晶片局拍照圖



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研究領域

數位 / 混合信號積體電路、通訊積體電路設計、生醫電子系統。

Abstract

In this information age, human interface devices such as display screens and speakers increases with the ever growing amount of information consumed. Conventionally, these devices are connected together by cables which can be ugly and clumsy, even causing trip hazards. Do you wish there is a better way to transmit this ever growing amount of information? High speed wireless communications is the answer!

By using the 60GHz transmission band, we can achieve higher transmission rate because of the wider available bandwidth, however this high transmission band is accompanied with other problems. The IEEE standards for 60GHz band(ie. IEEE 802.15.3c and IEEE 802.11ad) provides for more than 1Gbps data throughput for links within 10 meters in distance. Both standards cover two modes of transmission, which are Single Carrier (SC) and Orthogonal Frequency Division Multiplexing (OFDM). The maximum tolerable non-ideal channel effects stated in these two standards are used as design criterions in this work. By doing so, we meet the requirements of both standards with just a single set of hardware. Our design is a standard-cell based implementation of a baseband receiver that thoroughly compensates the non-ideal channel effects, therefore reducing the system bit error rate while maintaining compatibility between both standards and both transmission modes (ie. a total of 4 types of transmission). The architecture of our design is deeply pipelined to enable a high operating frequency. This high operating frequency coupled with an 8x parallelism of the data-path, maximizes the processing power of our design to support up to 24 Gbps data throughput, which is more than twice the transmission rate of HDMI (ie. 10.2Gbps). Besides, our design boasts a low gate count and low power consumption.

In this design, we propose a new channel estimation concept: Window-base Noise Cancellation (WNC). This algorithm cancels the error caused by noise during channel estimation to provide a more accurate channel estimate. It reduces the mean square error (MSE) of the equalized symbols by 33.58dB, providing the system the ability to achieve 64-QAM modulation, which is difficult for other systems to achieve. Together with a large modulation alphabet size, our high performance baseband processor achieves the high transmission rate which is not easily achievable by other systems.

Our cell-based design implementation includes RTL coding, logic synthesis, place & route, and layout merge. This design flow includes a massive amount of verification to ensure the correctness in each stage. These verifications cover function, timing, power, DRC, LVS, and IR drop. The design of this communication baseband receiver includes many modules, therefore it is a big challenge to integrate the different modules and to verify the correctness of each module with different tools. We use the EDA tools provided by CIC, and work on every detail to produce the best performing design.

Regarding the measurement results, the chip can run at 417 MHz with 496.39 mW when the Core VDD is 0.9V. The result can match our target of proposal which is 20 Gb/s. If increasing Core VDD to 0.94V, the chip can run at 500 MHz with 697.8 mW. These results show that the design can be used on high definition multimedia and indoor short distance transmission. It can make the home environment more convenient and clean.

Process	40 nm CMOS GP process, 1P9M
Supporting standard	IEEE 802.15.3c WPAN /802.11ad WLAN
Supporting mode	OFDM
Core size	1.59 mm^2(2.45 mm x 0.653 mm)
Die Size	7.77 mm^2(3 mm x 2.59 mm)
Gate count	1407 K
Operating frequency	417 MHz, 0.9V 500 MHz, 0.94V
Chip rate	3336 GS/s, 0.9V 4000 GS/s, 0.94V
Power Consumption	496.39 mW@417 MHz 697.8 mW@500 MHz
Throught rate	20 Gb/s @ 417 MHz (64QAM) 24 Gb/s @ 500 MHz (64QAM)

Fig.2 / Fabrication results of proposed baseband receiver