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Iterative Detection and Decoding Receiver for LDPC-Coded MIMO Systems

適用於 LDPC 編碼多天線系統的疊代式接收器

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作品摘要

研究動機：

行動裝置使用人口日益增加，無線資料傳輸需求也隨之提高。多天線技術（MIMO technology）可增加資料傳輸量與提升資料可靠度，已被現今通訊標準所採用。為了使傳輸資料達到 Shannon 極限，可使用 LDPC 編碼的 MIMO 系統搭配疊代式檢測與解碼接收機（Iterative detection and decoding receiver，IDD receiver），然而疊代式接收機面臨高複雜度、運算時間過長的設計挑戰，被認為未達實用階段，至今尚未被現有系統所採用。本作品提出文獻上第一顆實現高速且低複雜度多天線系統疊代式接收機，為通訊技術上之一大突破。

系統架構：

1. 傳統接收機在 MIMO 檢測器收到訊號後直接傳送至 LDPC 解碼器。疊代接收機設計為 MIMO 檢測器與 LDPC 解碼器之間進行訊息疊代交換，以較可靠之接收訊息更正較不可靠的訊息，可有效降低系統錯誤率。
2. 原本疊代式接收機在 MIMO 檢測器與 LDPC 解碼器之間來回交換訊息，具有較低硬體使用率與較長運算時間。本作品採用交錯解碼的排程，依序接收兩個碼框，分別運行在 MIMO 檢測器與 LDPC 解碼器，以此提升接收機吞吐量、提高硬體使用效率和縮短運算時間，將硬體使用率提升至 100%。
3. 最佳的 MIMO 檢測器為 MAP（Maximum a posteriori）檢測器，但 MAP 複雜度太高，在硬體實現上幾乎可不行。我們採用硬體複雜度較低之 MMSE-PIC 檢測器，透過疊代式解碼的更正錯誤能力，所實現的 MMSE-PIC 疊代式接收機較 MAP 非疊代式接收機具有更好的錯誤率效能。

硬體突破性：

1. MMSE-PIC 檢測器需要複雜之反矩陣計算，本作品使用可擴充式之矩陣拆解演算法結合矩陣轉換，將其轉換為上三角矩陣算用，並以低複雜度之 CORDIC 架構，只需要位移器和加法器即可實現，省去硬體複雜度高的除法器，以達成高速吞吐量。
2. 設計 MMSE-PIC 檢測器與 LDPC 解碼器資訊交換介面，本作品改變資訊更新方式，從 LDPC 解碼器的後驗機率（a posteriori probabilities，APPs）記憶體提出資訊與 MMSE-PIC 檢測器的資訊運算，再存回後驗概率記憶體，節省原本要傳給 LDPC 解碼器大量更新記憶體（31,104 位元），以較少硬體複雜度達成相同錯誤率效能。
3. 本作品採用 MMSE-PIC 檢測器與 LDPC 解碼器外部資訊交換之最佳疊代組合，具有最大邊際效能改善與最小額外增加硬體複雜度，比非疊代式接收機有 1.6dB 增益，邏輯閘數為 998k。

實作結果：

本作品提出之疊代式接收器以 40nm CMOS 製程實現，晶片面積為 1.33 mm^2，最高工作頻率為 288 MHz。在 4x4 16-QAM 系統可達到 794 Mb/s 的吞吐量。操作在 0.9V，晶片功耗為 135 mW，能量效率為 170 pJ/bit。本作品提出之疊代式接收器錯誤率效能超越最佳非疊代式接收器，能量與面積效能甚至高於現有之非疊代式接收器，所提之硬體架構與設計方法可直接應用於現有與未來之無線通訊接收機設計，極具產業效益。

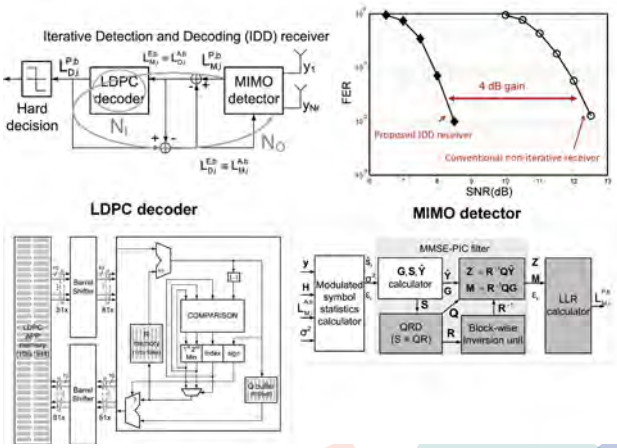
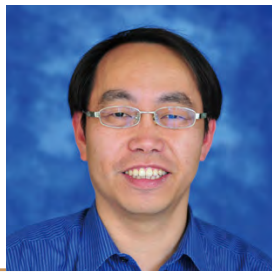


圖 1 / 疊代式接收機系統方塊圖、設計圖與錯誤率效能



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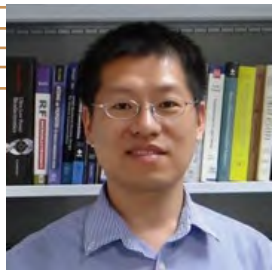
1997 年畢業於臺灣大學電機工程學系，並於 2001 年在同系獲得博士學位。畢業後於工業界從事藍芽和 PHS 基頻晶片研發 4 年，現任教於清華大學。近五年以第一或通訊作者的 IEEE 期刊論文有 16 篇。很榮幸獲頒 101 以及 102 清華大學產學合作績優獎項。

研究領域

編碼理論、無線通訊系統以及通訊 IC 設計。



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楊家驤教授於 2002、2004 年畢業於臺灣大學電機工程學系與電子工程學研究所，並於 2010 年獲得加州大學洛杉磯分校電機博士學位，隨後在加州大學洛杉磯分校擔任博士後研究，在 2011 年加入交通大學電子工程學系任教至今。

研究領域

生醫訊號處理與晶片設計、通訊系統與積體電路設計、低能耗電路。

Abstract

Motivation

In order to handle more mobile users, there is a strong demand for high-speed wireless communication systems. Multi-input multi-output (MIMO) technology has been widely adopted to support higher speed and more reliable data transmission. A low-density parity-check (LDPC)-coded MIMO system with iterative detection and decoding (IDD) receiver can achieve near-capacity performance. A practical IDD receiver, however, is still regarded infeasible due to its prohibitively high computational complexity and lengthy latency. In this work, we propose the first true IDD receiver with an MMSE (minimum mean-square error) based MIMO detector and a LDPC decoder to support high throughput with minimized area. Compared with conventional receiver, this work has better FER (frame error rate) performance, the optimal area efficiency and energy efficiency.

System model

1. For conventional non-IDD receiver, the decoder outputs the information bits without feeding the soft information back to detector. In an IDD receiver, in contrast, a MIMO detector and LDPC decoder iteratively exchange soft messages represented by the log-likelihood ratio (LLR) for each code bit.
2. IDD receiver is hard to implement due to high computational complexity and length latency. In our design, an efficient interface scheduling is proposed. The hardware utilization can be improved by 2 interleaved frames that yield 100% utilization with a minimized latency.
3. The optimal MIMO detector such as MAP (maximum a posteriori) detector is regarded infeasible as a result of high computational complexity. An MMSE-PIC (parallel interference cancellation) based IDD receiver can achieve the better FER performance than MAP based conventional receiver. This demonstrates a low-complexity MMSE-PIC detector is sufficient for IDD receiver, which can be leveraged to reduce detector complexity, especially for large-scale MIMO systems.

Breakthrough

1. MMSE-PIC detector needs to process inverse matrix operation that reduces the hardware throughput. To enhance the throughput with minimized area, QR decomposition (QRD) is utilized to facilitate matrix inversion needed in the MMSE-PIC algorithm by leveraging the characteristic of the upper-triangular matrix.
2. The messages are updated based on the turbo principle for IDD. In the direct-mapped design, the LDPC decoder requires an additional memory for LDPC intrinsic memory to store the LLR difference. In the work, an efficient interface is proposed to reduce hardware complexity. The messages are updated only when the detector produces the LLR difference, saving 31,104 bits for memory storage.
3. Based on the tradeoff between hardware complexity and FER performance, Outer iteration and inner iteration can be determined through sensitivity analysis. In this work, outer iteration and inner iteration are equal to 3 respectively that is adopted to achieve the optimal operation, where a gain of 1.6 dB over the base-line MMSE-PIC non-IDD receiver is achieved.

Experimental Results and Conclusion

A LDPC-coded MIMO systems with IDD chip is integrated in 1.33mm^2 in 40nm CMOS. The maximum gross throughput is 794Mb/s for a 4x4 16-QAM configuration at 288MHz. The chip dissipates 135mW at 0.9V, achieving an energy efficiency of 170pJ/bit. The proposed MIMO detector, LDPC decoder, message exchange interface, and outer-inner loop optimization for the IDD receiver can be applied to existing and future communication systems to enhance transmission performance.