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A Mixed-Signal Beamforming and Precoding Processor for mmWave Systems

適用於多輸入多輸出毫米波系統之混合訊號波束集成及預編碼處理器

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作品摘要

在第五代行動通訊（5G）中，為提供高速的傳輸速度，我們需更寬大的傳送頻寬。然而，現今低頻的頻譜擁擠程度，使往極高頻發展成為難以避免的趨勢。因此在 5G 通訊中，毫米波無線通訊系統經常被廣泛討論，而如何針對毫米波通道特性進行演算法和硬體設計將會是個關鍵議題。

毫米波無線通訊系統能在短距離的傳輸中，提供高資料流的傳輸。由於毫米波的波長較小，使得傳輸端與接收端能使用較大量的天線傳輸資料，減輕毫米波訊號衰退較強所造成的影響。此外，藉由多資料流系統的預編碼的技術，能夠進一步的提升傳輸的品質。然而，因毫米波系統能使用較多的天線數目，使得射頻電路的複雜度也隨之提高。為了降低硬體的複雜度，預編碼處理可由類比和數位電路的間接處理，而以較低複雜度的電路來實現。

此研究提出了新的射頻 / 基頻預編碼系統之建構方法，不僅減少了原先預編碼重建之演算法的運算複雜度，還能給予較高的硬體平行度。最後，此研究利用 TSMC90GUTM 製程來實作此研究提出的演算法之預編碼重建處理器。此處理器適用於 8x8 多輸入多輸出毫米波系統，能支援一至四個資料流的傳輸，共四種模式。根據晶片量測的實際效能，當電源供應為 1V，此處理器的操作頻率為 118 MHz，且功率消耗為 193.6mW。另外，此處理器的核心面積為 3.94 mm2。當資料流為一至四時，此處理器分別能在每秒運算 4.7 M、4.7 M、3.5 M、2.8 M 個不同的通道矩陣。

總結來說，毫米波和 Beamforming 的組合可以提升 throughput 和傳輸可靠度，此技術對於未來 5G 行動通訊將甚為關鍵。而如何兼顧運作效能和硬體複雜度更是實作上的重要課題。此外，本研究實作出世界第一個毫米波 Hybrid Beamforming 演算法之晶片，此成果對於 5G 的前瞻性研究有重大貢獻。

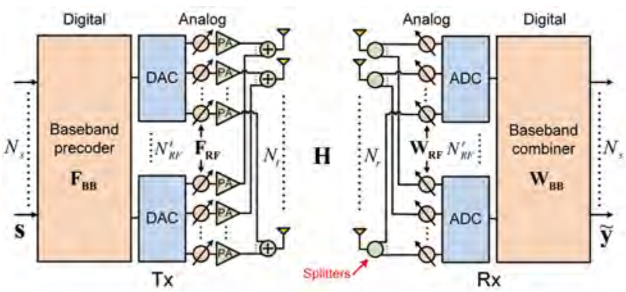

圖 1 / 混合類比數位預編碼系統方塊圖

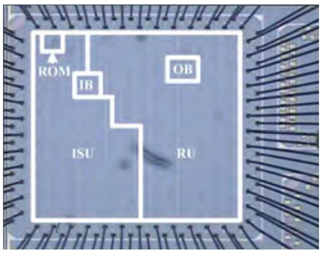

圖 2 / 晶片佈局照片

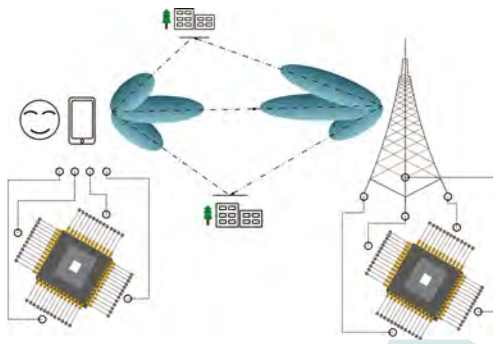

圖 3 / Beamforming 技術示意圖

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研究領域

無線通訊系統、通訊系統晶片設計、數位訊號處理晶片設計。

Abstract

In the fifth generation mobile communication system (5G), researchers seek more transmission bandwidth to support higher transmission speed. However, the scarcity of the bandwidth in lower frequency bands has made the pursuit for higher frequency bands as an inevitable trend. Therefore, mmWave wireless communication technologies have attracted many research attentions in the 5G system. Moreover, the designs in algorithms and hardware exploiting the mmWave channel characteristics will remain a critical issue.

A millimeter wave (mmWave) communication system provides multi-Gbps data rates in short-distance transmission. Because millimeter waves have short wavelength, transceivers can be composed of large antenna arrays to alleviate severe signal attenuation. Furthermore, the link performance can be improved by adopting precoding technology in multiple data stream transmission. However, the complexity of radio frequency (RF) chains increases when large antenna arrays are used in mmWave systems. To reduce the hardware cost, the precoding circuit can be jointly designed in both analog and digital domains to reduce the required number of RF chains.

This paper proposes a new method of building the joint RF and baseband precoder that reduces the computation complexity of the original precoder reconstruction algorithm and enables highly parallel hardware architecture. Moreover, the proposed precoder reconstruction algorithm was designed and implemented using TSMC 90 nm UTM CMOS technology. The proposed precoder reconstruction processor supports the transmissions of one to four data streams for 8 × 8 mmWave multiple-input multiple-output systems. According to the measurement results, the operating frequency of this chip was 118 MHz and the power consumption was 193.6 mW when the supply voltage was 1V. The core area of the post-layout result was about 3.94 mm2. The proposed processor achieved 2.8 M, 3.5 M, 4.7 M, and 4.7 M channel matrices per second in four-, three-, two-, and one-stream modes, respectively.

In conclusion, the combination of the mmWave properties and the beamforming technology can achieve higher throughput and reliable transmission. It is a significant technology for the next generation (5G) mobile communication system. Additionally, the balance between performance and hardware complexity remains a substantial topic in implementation. Finally, this study implemented the first chip in the world based on the mmWave Hybrid Beamforming algorithm. It has made a major contribution to the future researches in the 5G system.

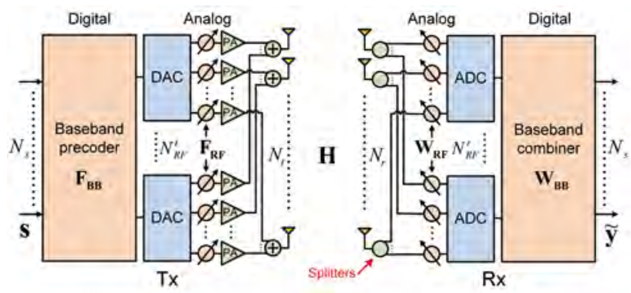

Fig.4 / System block diagram of the joint RF/baseband precoding in an Nt × Nr mmWave single-user system with Ns data streams

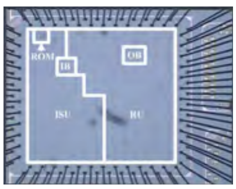

Fig.5 / Chip Layout

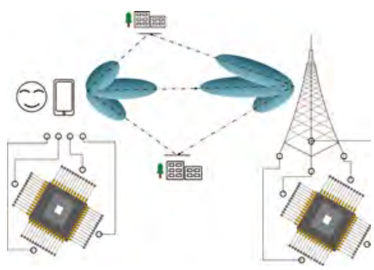

Fig.6 / Beamforming technology diagram