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Design Group

應用於超低待機功耗非揮發性處理器之非揮發性邏輯電路
Energy Efficient Nonvolatile Logic Used in Nonvolatile Processor

隊伍名稱　太陽的後翼 / The Solar Wings
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研究領域：記憶體積體電路設計、非揮發性邏輯電路、computing-in-memory, memory-based deep learning circuits。

作品摘要

隨著穿戴式裝置與無線傳輸系統近年發展，物聯網（IoT）與無線感測網絡（WSN）成為熱門技術開發。然而，隨著應用系統節能與能源不穩定問題，長待機時間與低耗能的特性為目前系統開發熱門議題。為了降低處理器待機時的大量耗能，非揮發性記憶體（nonvolatile memory, NVM），如快閃式記憶體（FLASH）、鐵電隨機存取記憶體（FeRAM）、電阻式記憶體（ReRAM）... 等由於其記憶特性，被用以備份處理器待機時資訊，並在復機後將資訊重新使用，如此就能大幅減少傳統揮發性（Volatile）記憶體待機時的漏電問題，並且有效改善能源利用。

傳統處理器（Conventional processor）由靜態隨機存取記憶體（SRAM）記憶體與電路正反器（Flip-Flop）等邏輯電路組成，為達到節省系統待機耗能，傳統解決方法採用 SRAM+NVM（2 macro solution）於待機時將資料備份至非揮發性記憶體（nonvolatile memory, NVM）中備份。然而，此種處理器與巨集間資料搬運的傳輸架構，在備份時搬動資料需要消耗大量能量，且受限於傳輸介面的輸入輸出端（IO）數，導致復機時資料搬動的時間和耗能隨著容量的增加而變得更為嚴重。

利用具有高密度、高低阻態比值（R-ratio）大的電阻式記憶體（ReRAM）與 CMOS 邏輯電路相結合，將非揮發性靜態隨機存取式記憶體（nvSRAM）與非揮發性正反器（nvFF）納入處理器應用，有別於傳統 2 Macro solution，此研究成功設計出在單一晶片可進行運算與資料儲存的電路架構，解決傳統處理器待機漏電的耗能並能從睡眠中快速喚醒儲存資料。更者，由於處理器中關鍵運算單元使用的暫存器由 nvFF 取代，處理器於復機後能接續執行關機前的運算，而不須重新執行，因此可以有效提升處理器運算效率。

本研究提出一 7T1R nvSRAM 與其輔助備份機制，Self-Write-Termination 與 Adaptive Parallel Decoder & Space Domain Controller 等周邊控制電路，並且提出一創新非揮發性邏輯電路 SWT-nvFF。

1. Adaptive Parallel Decoder & Space Domain Controller 可以針對資料使用情形，大幅降低 nvSRAM 巨集的備份耗能。

2. 創新的 SWT-nvFF 達成最小的 D-Flip Flop 面積增加率，並大幅降低資料備份耗能。

本研究使用 65nm CMOS 製程進行晶片實作驗證提出的架構與電路，並將提出的 nvSRAM 巨集架構與 SWT-nvFF 整合於處理器系統中，製作出新型態的非揮發式處理器，以下為非揮發式處理器的特色。

1. 應用於一實際微處理器並成功達成處理器於復機後能接續執行關機前的運算。

2. 解決揮發性電路待機漏電耗能問題，在關機前只需將資料備份即可關閉電源並在開機前回存資料，並等待周邊邏輯電路恢復功能，達到快速、低耗能開關機特色。

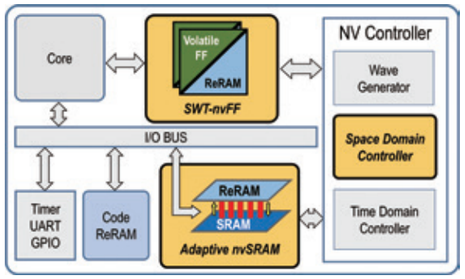

圖 1. 感測器架設位置 / Fig 1. Strucure of one macro nonvolatile Processor

Abstract

In recent year, according to the development of wearable device and wireless transmission system, the Internet of Things (IoT) and Wireless Sensor Network (WSN) related technologies become popular. However, due to the low power requirements in system and the unstable power source, the features of the low power and long standby time become the hot topic now. In order to reduce the power waste at standby mode in processor, Nonvolatile Memory (NVM), such as Flash, FeRAM, ReRAM were used to back up the critical data before shut down the system and reuse it after wakeup. As a result, the leakage power during standby mode of volatile system can be reduced to achieve more efficient power usage.

Conventional processor is based on SRAM、Flip-Flop and various other logic circuits. To achieve energy saving, two macro solution were normally used. Two macro solution is constructed by SRAM and NVM macro, NVM can save data from SRAM even the supply power is turned off. However, due to the limitation of the IO amount of the macro transmission interface, this method requires large power consumption during data transmission between two macro.

By using high density and high performance ReRAM combined with CMOS process, this project propose one macro solution of nonvolatile SRAM (nvSRAM) and nonvolatile Filp-Flop (nvFF). Compared with conventional two macro solution, nvSRAM and nvFF have few benefits, one for leakage reducing during standby mode, second for decrease power consumption during data backup/restore, and third for fast system reboot.

This project propose a nvSRAM Macro containing several assisting backup/wakeup schemes, Self-Write-Termination (SWT), Adaptive Parallel Decoder & Space Domain Controller. Also, a novel of Self-Write-Termination nvFF (SWT-nvFF) is proposed in this project.

1. Adaptive Parallel Decoder and Space Domain Controller circuits provide an excellent solution for reducing backup and restore power consumption.

2. SWT-nvFF comply the smallest area overhead compare with other nvFF, and greatly reduce power consumption for data backup.

Finally, by using 65nm CMOS fabrication, the proposed schemes has been verified. Furthermore, as the following, our proposed schemes were also implemented within a processor to achieve a nonvolatile Processor feature.

1. Application of proposed scheme within a MCU was implemented. This processor can continue all processing missions between each standby/wakeup mode switching.

2. To solve standby leakage issue of volatile circuit, nvProcessor can store the data within embedded NVM during the standby mode prevent from data loss, then the power source can be turned off. After waking up the system, the stored data can be immediately restored to the logic circuits. This method provides processor consume Zero power consumption during the standby mode.