D16-042
Design Group

使用休眠切換技巧之超低功耗類比數位轉換器
Ultra Low Power SAR ADC with Semi-resting DAC

隊伍名稱　偷休息省電 ADC / Semi-resting ADC
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研究領域：CMOS 影像偵測 IC 設計、低壓低功耗類比數位轉換器設計、類比前級電路設計、智慧型影像應用單晶片設計、生醫應用影像感測 IC 設計、類比與混波 IC 設計。

作品摘要

在物聯網的應用下，我們需要具有高能源效率的數位類比轉換器，並具有中等的操作速度和解析度。逐漸趨近式類比數位轉換器（SAR）在全球近幾年藉著提升電容陣列（DAC）切換效率和低功耗比較器的演進，靠著低電壓 SAR 展現了非常好的能源效率表現。為了要在更進一步降低電容陣列功耗，很多降低電容陣列功耗的方法被提出，但分別都有造成需額外電壓源、兩段式操作、或著是 reset 功耗為代價。為了降低比較器功耗，多次比較或著是二階式的 ADC 被提出，但都付出了複雜的周邊電路為代價。在降低電壓節省功耗的趨勢中，ADC 能達到的解析度，也被訊號範圍相對縮小所限制住。

在此晶片中，此晶片提出了休眠電容陣列、串接式比較器、和雙倍輸入訊號範圍的技術來解決上述問題。圖一為此晶片的 ADC 架構，使用了兩個十位元的 AD_0 和 AD_1。兩個 ADC 分別處理不同範圍的輸入訊號輪流休眠，可用的輸入訊號範圍因此提升到 ±2Vdd，在此晶片即是在 0.3V 供電的情況下有 ±0.6V 輸入範圍。使用了休眠切換技巧，利用電荷直接中和的特性進行第一次切換即可以不消耗能量進行第一次切換。剩餘的切換，可以靠著低壓 MCS 的切法完成而達到絕佳的能量消耗。最後本設計提出了，更改傳統兩級比較器的架構，將其第一級改成 MOS 串聯疊加的方式，比較器可以得到三倍的增益，相較起傳統的比較器本設計只需要消耗 49% 的功耗和 66% 的比較時間，就可以達到一樣的雜訊品質。

本晶片使用 90 奈米的 CMOS 製成，面積總共是 0.0354mm^2（295μm×120μm）如圖二所標。此 ADC 是 11 位元的 ADC，操作在 0.3V 且有 600KS/s 的取樣速度。其最大 DNL 和 INL 的規格分別是 +0.37/-0.63 和 +0.72/-0.71LSB。在 Nyquist-rate 的輸入訊號下，量測到的 SNDR、SFDR、ENOB 分別是 58.71dB、73.35dB、9.46 位元。靠著提出的休眠電容陣列、串揭示比較器、和雙倍輸入訊號的方式，此架構在 0.3V、600KS/s、11-bit 的情況下達到了 FoM 為 0.44fJ/conv-step 的規格。圖三是發表在 ISSCC 和 VLSI 上的論文，他們的 FoM 和操作速度的關係，可以看到此設計在量測上，達到了比世界最省電之 ADC 還要在更加省電一倍的規格。

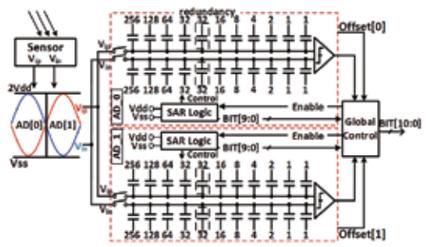

圖 1. 本設計架構圖 / Fig 1. The architecture of proposed SAR ADC

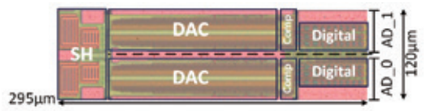

圖 2. 晶片局部照相放大圖 / Fig 2. micrograph of proposed SAR ADC

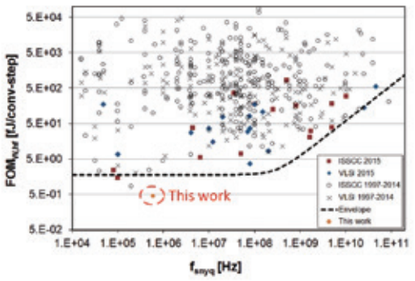

圖 3. FoM 對應取樣頻率 / Fig 3. FoM versus the sampling frequency

Abstract

Internet-of-everything (IoE) applications require high energy-efficient ADC with moderate sampling rate and resolution. Successive-approximation register (SAR) architecture demonstrates a convincing and improving performance in recent years with technical developments of DAC switching and low-power comparator in a pushing-down supply operation. For DAC switching energy reduction, many works were reported with design tradeoffs including requirements of extra reference voltage, sub-ranging operation, and reset energy. For comparator power reduction, majority voting and hybrid SAR ADC were proposed with penalties of complex critical-decision-detection and calibration-supporting circuits. With a lowering-down operational supply, the achieved performance and application of ADC are limited due to the degraded signal swing as well as the decreasing LSB.

This work presents a new SAR ADC architecture with semi-resting (SR) DAC, cascade-input (CI) comparator, and double rail-to-rail range to solve the issues. Fig. 1 shows the architecture of the proposed 11b SAR ADC composed of two 10b (AD_0 and AD_1). The AD_0 and AD_1 are designed to handle different input range. The total input range is effectively doubled to ±2Vdd, which is ±0.6V at 0.3V supply in this work. By performing proposed SR switching procedure, the bottom plates of AD are merged together by charge averaging operation without consuming any switching energy after the MSB comparison. The remaining conversions of MSB-2 to LSB are accomplished in a MCS-based operation to achieve ultra-low switching energy consumption. With proposed cascade-input (CI) comparator, the effective front-stage gain of two-step comparator is increased by 3-x with a 3-stacking cascaded input pair in this design. Compared to the conventional noise reduction approach, the CI comparator consumes only 49% of power and 66% of decision time to achieve the same noise performance.

A prototype chip is fabricated in 90 nm CMOS with a core area of 0.0354mm^2 (295μm×120μm) as shown in Fig. 2. The static and dynamic performance of the implemented 11b ADC with a 0.3V supply and 600KS/s. The DNL and INL are +0.37/-0.63 and +0.72/-0.71LSB, respectively. With a Nyquist-rate input, the measured SNDR, SFDR, and ENOB are 58.71dB, 73.35dB, and 9.46-bit, respectively. With the proposed SR DAC, CI comparator, and corresponding design for low-voltage operation, the implemented 0.3V 600KS/s 11b ADC achieves a FoM of 0.44fJ/conv-step. Fig. 3 shows the FoM versus the sampling frequency compared with state-of-art works, the achieved FoM performance is lowest, which is only half of the best-reported result.