D16-051
Design Group

應用快速收斂技術之兩百億位元可適性線性等化器
A 20Gbps Adaptive Linear Equalizer Using a Fast-converging Method

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研究領域：類比 / 數位積體電路、鎖相迴路及延遲鎖定迴路、通信積體電路、混合式及射頻積體電路系統、微感測器積體電路、類比數位轉換器。

作品摘要

現今，隨製程技術的演進及 I/O 介面的成本考量，有線通訊系統正朝向串列資料傳送的架構發展，即 Serdes 架構。然而，當串列資料的速率日益增加，對於系統頻寬的要求也越來越高，此時通道損耗的效應將無法再被忽視。通道損耗的效應來自於傳輸資料媒介的非理想性，如印刷電路板常用 FR-4 或 Rogers 等板材，基板本身由環氧樹脂（Epoxy）等介電材質所組成，而非理想的介電係數將造成資料高頻成分的衰減；另外，通道材質也會依不同金屬材質有不同的集膚深度，同時也會衰減高頻資訊分量。

上述通道損耗效應將造成時域上明顯的符際干擾，即 ISI，此效應對於接收機前端類比電路而言，會造成可觀的錯誤判斷，累積巨大的誤碼率（BER），因此，有線通訊系統中需置入等化器（Equalizer）以補償此損耗的效應，而置於接收端的等化器對於未知的通道特性需具備有適應性（Adaptive），能自動偵測並調整所需補償的增益，以達到最佳的資料眼高（Eye-height）與抖動（Jitter）。

本研究旨在提出一個有別傳統的適應性演算法，並驗證於一操作在 20Gbps 的線性等化器。此可適性系統具備四項優勢：其一，不需憑藉時脈資料回復電路（CDR）提供高速且同步的時脈訊號，除可避免雙迴路的穩定性議題與降低電路設計時的複雜度外，亦可省下 CDR 系統的穩定時間（Settling time）。其二，不需置入類比濾波器以分離資料中高頻與低頻的分量，如此可避免製程變異對於被動元件的影響。其三，採用非同步取樣，且前景數位電路校正的方式，除可克服 PVT（Process/Voltage/Temperature）變異外，同時也適用於先進製程中。最後，我們所提出的適應性演算法具有使等化器係數快速收斂的特性，可滿足多數通訊系統的規格要求，間接提供了功率消耗與收斂時間互為折衷的一種解決方法。

此具備適應性的線性等化器系統實現於 40 奈米低功耗 CMOS 製程，操作電壓為 1.1 伏特，共消耗 12.8 毫瓦，其中，線性等化器消耗 7.9 毫瓦，可適性系統消耗 4.9 毫瓦。系統驗證於三條不同長度的 FR-4 通道，實驗結果顯示此系統最大能夠克服 18.3 dB 的通道衰減，而等化器係數收斂時間僅約 2.68 微秒，較先前技術縮短要一倍以上的時間；另外，性能指標 (FOM) 為 0.035pJ/bit/dB，優於現有文獻三倍以上。實際量測的結果顯示此演算法實現於補償高速資料傳輸時損耗的可行性及優勢，可應用於現階段 USB3.0、USB3.1、PCIe Gen3 等市面常見的有線通訊系統，甚至能夠符合未來更寬頻操作、更低功耗需求、更短系統穩定時間等通訊系統規格。

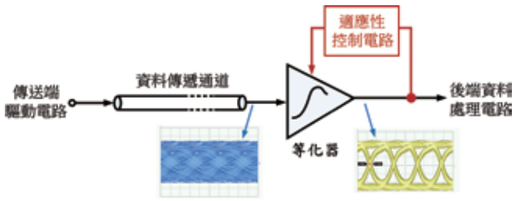

圖 1. 有線通訊系統類比前端具備適應性等化器

Abstract

As the required speed of several wireline applications grows, the channel dispersion caused by the skin effect and dielectric loss becomes increasingly worse. The received data suffers from the significant inter-symbol interference (ISI), and thereby the bit error rate (BER) deteriorates. To properly compensate the ISI for different channel characteristics, various adaptive methods for the linear equalizer are presented. Owing to the lossy channel, the high-frequency components of the data get attenuated and the power of high-frequency components would be smaller than that of low-frequency ones consequently. The adaptive equalizer is used to make both of them equal by averaging, or doing statistics of the received data. To collect the information requires a certain period of time and thereby leads to a long adaptation time of the equalizer.

However, the adaptive equalizer with a short adaptation time is in high demand for the data transceivers. That is because the shorter adaptation time leads to the faster initialization of the overall data communication systems. Although the adaptation time can be reduced by using high-speed circuits, the huge power consumption may be required and the power efficiency of the whole system is decreased accordingly. In summary, the conventional methods suffer from the trade-off between the power consumption and the adaptation time.

In this work, the magnitudes of the received data is directly compared with the predefined level. The adjustment of the linear equalizer is divided into two parts: high-frequency and low-frequency gain adaptation. To reduce the asynchronous sampling time, the high-frequency gain is calibrated prior to the low-frequency one. Then, the magnitudes of high-frequency and low-frequency components are ultimately equal. Furthermore, the power consumption of the proposed method based on the asynchronous sampling technique can remain within an acceptable range while the data rate is higher than 10-Gb/s.

Fabricated in 40-nm CMOS technology, this linear equalizer totally consumes 12.8mW from 1.1V supply, of which only 4.9mW dissipates in the adaptation logics. With a 20-Gb/s PRBS7, the measured bit error rates are all less than 10-12 for channel loss from -7.8dB to -18.3dB. Moreover, the adaptation time is aggressively reduced to 2.68us, which is a remarkable improvement as that in the recent works. The calculated figure-of-merit (FOM) is 0.035pJ/bit/dB, which is also one-third compared to other adaptive equalizers. Above all, the proposed method mitigates the trade-off between the adaptation time and the power consumption of the adaptation logics.

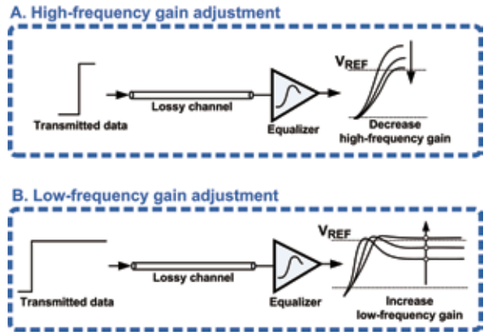

Fig 2. Adaptation procedure