設計組
Design Group

D18-061

以頻率鍵移調變實現之極低功率收發機

A 0.6-V 200-kbps 429-MHz Ultra-low-power FSK Transceiver in 90-nm CMOS

隊伍名稱　無遠弗接 Always Catch You
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研究領域

生醫應用高能量效率無線通訊晶片、電源管理晶片、應用於PLL與Delta-Sigma ADC之混合信號電路設計技術、感測器與生醫應用類比訊號處理電路。

作品摘要

近幾年隨著無線技術持續進步下，強調低功率之無線技術主要有第四代藍芽（Bluetooth Low Energy, BLE）和ZigBee兩種規格，其市售IC消耗電流約為10~20毫安培，需要電池來維持工作，但在許多應用中，頻繁更換電池的需求相當不便。如圖一所示，未來於物聯網（Internet of Things, IoT）或人體植入式醫療應用上，以不安裝電池的方式，來達成傳輸與接收資料，將會是無線通訊上重大突破。因此，設計極低功率之無線收發機是相當重要的環節。以超低供應電壓來設計無線發射機，來減少能量收集電路的升壓次數，提升電路功率轉換效益 。

本作品提出之電路架構如圖二所示，結合了多種電路架構與相關技術，各取其所長並結合而成，相較於過往的作品，有以下特點：

1. 透過頻率鍵移調變的方式，相較於相位或振幅鍵移調變，更能忍受相鄰通道所帶來的干擾，但在電路複雜度及功耗上，付出額外的代價。但藉由提出之類比方式進行解調，相比於現有數位解調，更能實現低功耗的願景，彌補頻率鍵移調變於功耗上所帶來的劣勢。

2. 為實現不具功率放大器的發送機架構，必須要克服壓控震盪器面對天線負載下，不易維持振盪的難題，而藉由採用阻抗匹配網路來取代功率放大器，把功率直接轉換到天線負載，此番難題將迎刃而解。

為了更具體理解阻抗匹配對發送機的不可或缺性，整理出以下三個重點：首先它可以直接當成雙端轉單端電路。其二，避免輸出負載為天線時，所導致的振盪器輸出阻抗增加。其三，以不增加整體系統元件個數，節省了電感和功率放大器於晶片實現的面積，精簡晶片大小。

最後歸納本次電路主要能省電的兩項原因：第一，發射機輸出處利用阻抗轉換到天線，可以省去功率放大器所造成大於58%的功率損失，大幅提高發射效率。第二，利用外部元件也可大幅減少震盪器功率消耗。

本作品以TSMC 90nm CMOS製程實現，收發機在0.6V的供應電壓之下，總共消耗0.536微瓦。接收機而言，當資料速率為200kbps時，輸入功率為-85dBm之位元錯誤率能控制低於千分之一；發送機而言，其消耗功率在0.39微瓦之下，輸出功率可達-8.19 dBm，整體效益為38.7%。

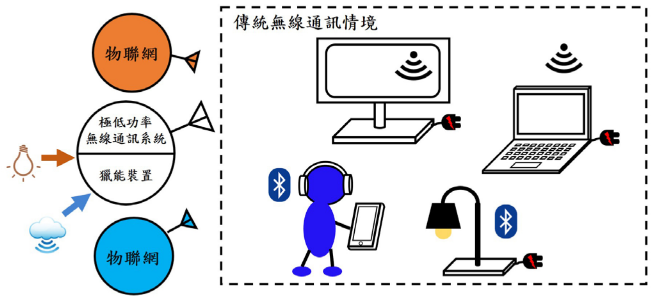

圖1. 物聯網概念

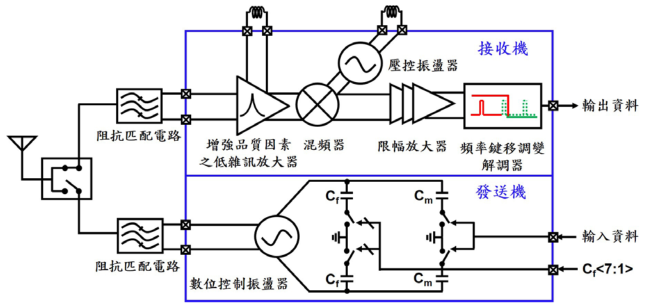

圖2. 本作品所提出之收發機系統架構

Abstract

Ultra-low power (ULP) transceivers (TRX) are important subsystems for Internet-of-Things (IoT) system. In these applications, due to restricted energy sources, a low-power and low-voltage radio is the target. Some examples of conventional wireless receiver (RX) and transmitter (TX), require several power-hungry circuits, such as low noise amplifier (LNA), phase-locked loop (PLL), power amplifier (PA), and analog-to-digital converter (ADC). The power consumption issue may be addressed in the injection-locked-based RX. However, to achieve effective injection, the swing of the injecting signal must be large enough, which consumes additional power.
For low-power consideration, it is an alternative mind to remove PLL and PA altogether. In this work, the proposed TX is essentially an open-loop voltage controlled oscillator (VCO) which drives the antenna via an impedance matching network for power conversion. The oscillation frequency can be adjusted via a frequency tuning loop. The TX global efficiency can be improved by removing PA.
The transceiver is fabricated in TSMC 90-nm CMOS process. The proposed RX achieves -85-dBm sensitivity at 0.1% BER and draws 0.146 mW. The proposed TX delivers -8.2-dBm output power and draws 0.39 mW. It achieves 38.7% global efficiency. To summarize above, this work presents an energy efficient thinking in FSK transceiver. Several circuit techniques are employed in this design.

1. To achieve better performances both on the sensitivity and power consumption, each of system parameters is well selected. As the result, the proposed TX and RX do not require a PLL to set the carrier frequency.

2. In the RX, the Q-enhanced LNA and low-power demodulator are proposed. By these ways, the sensitivity can be optimized in finite power budget.

3. In the TX, the VCO is directly interfacing with the antenna to eliminate the PA.

The measured RX achieves high sensitivity and low power consumption, which is manifested as Fig. 3 (red one); meanwhile, the TX accomplishes a good global efficiency, which is shown as Fig. 4 (red one). The proposed transceiver can be applied to energy-constrained IoT or biomedical devices.

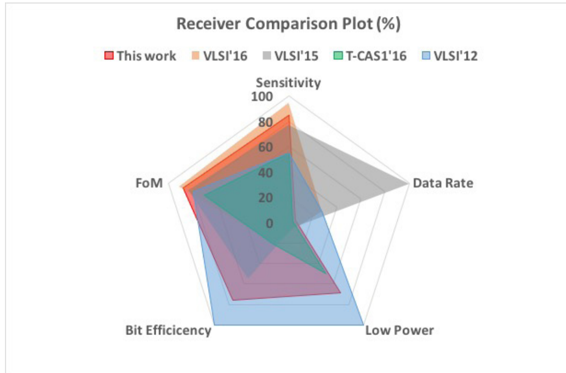

Fig.3 The receiver benchmark

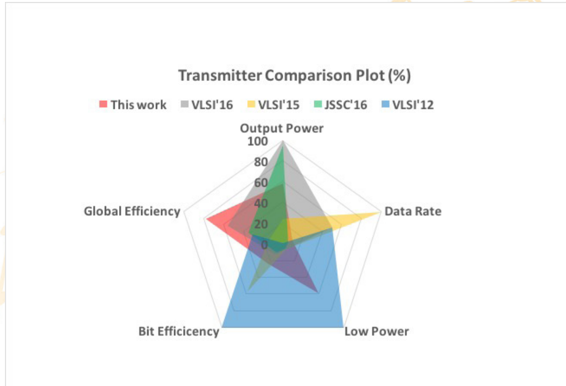

Fig.4 The transmitter benchmark