悠遊 5G 智領未來：毫米波 10 Gbps 吞吐率之單載波無線基頻傳收機晶片

D19-014

Cruise 5G-Intelligent Future: A Single Carrier mmW 10 Gbps Throughput Rate Wireless Baseband Transceiver Chip

隊伍名稱 5G 變形金剛
5G Transformer

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研究領域
數位/混合信號積體電路、通訊積體電路設計、生醫電子系統。

作品摘要

為了因應未來後 5G 時代傳輸資料率大幅提升的應用場景需求，毫米波（mmW）頻段將會扮演關鍵性的角色，透過毫米波高傳輸頻寬的特性，將可以提供數十 Gbps 等級的高資料率。目前 ITU 公佈了24 GHz 到 86 GHz 之間的全球毫米波頻帶清單，而現今 24 - 86 GHz 之主要研究在 40 GHz 以下之頻帶，因此本作品以 66 - 76 GHz 及 81 - 86 GHz 頻帶原主，以達到更高的傳輸速率。

圖一為本基頻傳收機晶片應用場景示意圖，目標為建構一個由固定式基地台及無人駕駛載具所佈建的 3D 空間通訊網路，透過 60 GHz mmWave 高速無線通訊技術、晶片，且結合多波束相位陣列天線，開發出高效率 60 GHz 傳收機電路 IC，最後透過 4G Cellular、Wi-Fi、Drone、以及光纖核心網路支援，便可達如天羅地網般的高寬頻與低延遲的未來智慧網路架構。而整個預期之 mmW 傳收機電路 IC 方塊圖如圖二，為了在未來能擴展至其他 mmW 頻帶及規格，硬體架構採用模組化設計，並且透過整合控制電路來完成更靈活的 mmW 無線傳收系統。為了達成模組化設計，RTL 撰寫時採用 IP 化設計，可隨意調整字長、平行度、暫存器級數等等，再利用控制電路及仲裁器來完成整個電路功能運行。

本無線數位基頻傳收機之晶片設計參考 60 GHz IEEE 802.11ad/ay 規格所制定的參數與框架架構，採用SC傳輸模式，目標的傳輸資料率為 10 Gbps，數位基頻電路的晶片速率（Chip Rate）從規格的 1.76 GHz 提升至 2.5 GHz。其中包括了外傳收機與內傳收機，不但可以補償、消除 60 - 86 GHz 環境下的非理想效應，還可以進行錯誤更正碼的編解碼，來進一步提升基頻傳收機的效能，且在傳輸資料率為 10 Gbps 時，效能可以達到規格的要求。

基頻電路實現使用 28 nm 製程下線，其中還整合了數位類比轉換器與類比數位轉換器來減少所需的接線，另外在與媒體存取控制層的接面以及與 DAC/ADC 的接面皆考慮了同步與協定的問題。而整體數位基頻電路採用四倍平行電路，最高的數位時鐘頻率為 625 MHz。最後在台灣半導體研究中心使用 ADVANTEST V93000 PS1600 自動測試系統證實功能完全正確。整個系統驗證使用整合性的印刷電路板及 NI Prototype 平台進行測試，可以將 MAC 層、類比電路以及前端電路加入一同進行 mmW 環境下對傳的效能驗證。延展性方面，此基頻架構可增加至 64QAM 及 8 倍平行就可輕易將傳輸速度達到 30 Gbps。

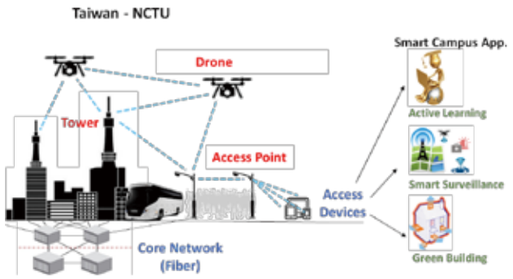

圖 1. mmW 基頻傳收機晶片應用場景示意圖

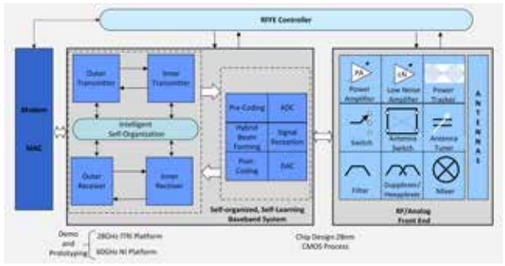

圖 2 . mmW 基頻傳收機晶片電路架構方塊圖

ABSTRACT

In order to meet the explosive growth of communication data rate demand in the scenario of future post-5th generation applications, the millimeter wave (mmW) is a key technology, which provides a wider transmission bandwidth and tens of Gbps data rate. Currently, International Telecommunication Union (ITU) has announced a global mmW band list of 24 GHz to 86 GHz, however, the recent research focuses on the band below 40 GHz. Therefore, this work target on the 66-76 GHz and 81-86 GHz band to achieve a higher transmission rate.

Fig.1 is the application scenario diagram of the proposed baseband transceiver chip. The target is to construct a 3D space communication network which is composed of immobile base stations and unmanned vehicles. Through the 60 GHz mmWave high-speed wireless communication technique and implemented chip, combining with multi-stream phase array antenna, a high efficiency 60 GHz transceiver IC is developed. Finally, with the help of 4G Cellular, Wi-Fi, Drone, and optical core network, a wide bandwidth and low latency smart network structure is able to be extensively constructed. The block diagram of the expected mmWave transceiver IC is as Fig.2. In order to expand the mmWave frequency band and extend to other specs, we adopt modularized design and integrate control circuits to all hardware architectures to accomplish a more flexible mmWave wireless transceiver system. For the sake of modularization, IP design concepts are adopted at RTL section, with flexible word length, parallelism, and pipeline stages of registers… etc. Eventually, we take advantage of control circuits and arbiters to complete whole circuit functions.

The chip design for the wireless digital baseband transceiver is based on the parameters and frame structure specified by the 60 GHz IEEE 802.11ad/ay standard. The proposed design adopts the single carrier (SC) transmission mode with a target transmission data rate of 10Gbps, and a chip rate of the digital baseband circuit increased from 1.76 GHz to 2.5 GHz. The overall architecture including the outer transceiver and the inner transceiver system does not only can compensate and eliminate the non-ideal effect in the 60-86 GHz environment, but it can also use the encoder and decoder for error correction to further improve the baseband transceiver performance. Furthermore, the chip performance can meet the specifications when operating at the data rate is 10 Gbps.

The baseband circuit has been implemented using a 28 nm process. The overall system includes a digital-to-analog and an analog-to-digital converter to reduce the required interconnections. In addition, the synchronization issue in the interface between the media access control (MAC) layer and the DAC/ADC has been also considered. The overall digital baseband circuit uses four times parallelism with the highest digital clock frequency of 625 MHz. Finally, the ADVANTEST V93000 PS1600 automatic test system was used at the Taiwan Semiconductor Research Center to verify the correct functionality. The entire system verification uses an integrated printed circuit board (PCB) and NI Prototype platform for testing. The MAC layer, analog circuit, and front-end circuit can be added together for performance verification in the mmW environment. With regard to the extensibility of this system, the baseband architecture can be increased to 64-QAM and eight times parallelism, making it easy to achieve 30 Gbps transmission data rate.