D19-020

使用 90 奈米技術之 90-100 GHz CMOS 毫米波單混頻器射頻收發機

A 90-100 GHz Millimeter-Wave Single-Mixer RF Transceiver in 90 nm CMOS Technology

DESIGN GROUP D19-020

隊伍名稱 翱翔於 100-GHz 天際的單混頻器射頻收發機
100 GHz Single-Mixer RF Transceiver

隊　　長 林新皓 / 成功大學電腦與通信工程研究所

隊　　員 周建彰 / 成功大學電腦與通信工程研究所

劉三賢 / 成功大學電腦與通信工程研究所

指導教授

莊惠如

成功大學電機工程學系

美國密西根州立大學電機博士，現為成功大學電機工程學系教授。曾任密西根州立大學工學院研究中心任博士後研究員、美國摩托羅拉公司無線電部門研究工程師。

研究領域

射頻 / 微波 / 毫米波無線通訊積體電路晶片 / RF-SoC、毫米波 vital-signs Doppler radar 晶片系統、無線通訊天線與被動元件、電磁數值計算及生物電磁之醫學工程應用、電磁輻射 / 干擾（EMI/EMC）計算測量。

作品介紹

本晶片利用 TSMC 90-nm GUTM CMOS 製程，設計一個 94-GHz CMOS 單混頻器射頻收發機毫米波晶片，發射端（Tx）及接收端（Rx）僅採用一個混頻器來做升降頻使用，中間再以 T/R switch 做切換，與傳統使用兩個混頻器（升頻與降頻）架構相比能省下一個混頻器及部分濾波器的使用，進而達到縮小晶片面積的功效。其晶片電路架構包含了射頻收發開關、功率放大器、低雜訊放大器及一可升降頻之單端次諧波電阻式混頻器，射頻收發開關之電路主體採用行進波概念開關之設計，將收發開關之導通電路等效成一人工傳輸線，利用行進波開關的特性達到寬頻響應和高隔離度特性，並搭配基極浮接與負基極偏壓技術改善插入損耗與線性度。功率放大器電路使用疊接式（cascode）架構，其具有承受較大之供應電壓、較好的增益及輸入與輸出級之間的隔離度等特性，整體以串接（cascade）五級達到較高增益，並且採用A類之偏壓形式來達較佳之線性度及功率增益特性。低雜訊放大器則採用疊接組態與共源極（common source）串接組態，利用串接五級電路將 94-GHz 微弱的輸入訊號放大至一定的水準，而為了更有效抑制雜訊，本次設計分別在前兩級電路間加入雜訊匹配電感以達最佳化雜訊之功用。而混頻器電路採用被動式單端次諧波架構來實現，其主要優勢在於此架構能同時具有升頻與降頻的功能，並擁有高線性度及零直流功耗等優勢。電路中之走線皆有透過適當彎折以達晶片面積之最佳利用，在佈局上皆採用M9當訊號線以減少訊號對基板的寄生電容所造成的損耗，直流偏壓走線則採用 M2、M3、M4 與 M6、M1 為接地面。整體功率消耗為 245 mW，晶片面積為 1.37 mm × 0.716 mm。本研製之 94-GHz 毫米波單混頻器射頻收發晶片將有助於提供一高整合性、低成本之收發機單晶片設計方案。

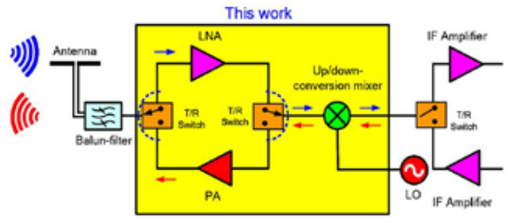

圖 1. 90-100 GHz CMOS 單混頻器射頻收發機毫米波晶片架構圖

圖 2. 90-100 GHz CMOS 單混頻器射頻收發機毫米波晶片圖。本毫米波射頻前端晶片，未來可用於5G NR 94-GHz 毫米波通訊及 IoT 的應用，另外還有應用於 94-GHz 毫米波 3-D 影像雷達來偵測隱藏在人體的武器

ABSTRACT

This work proposes a 90-100 GHz bidirectional RF front-end transceiver fabricated in 90-nm CMOS technology, in which the circuit complexity is reduced through the use of a single-mixer architecture. In general, if some of the circuit blocks of the transmitter (TX) and receiver (RX) chains can be shared, the opportunity exists to operate the transmitting and receiving modes in a time-division duplexing manner. For bidirectional RF transceivers (especially those with a large transceiver array), such an opportunity yields several important practical advantages, including a lower power consumption and a smaller chip size. As shown in fig.2, the single-mixer RF transceiver consists of two transmit-receive (T/R) switches, a power amplifier (PA),a low-noise amplifier (LNA), and a bidirectional sub-harmonic mixer. A T/R switch with the traveling wave technique is used for wideband response and low insertion loss, the traveling-wave concept is applied by adopting a distributed transmission line structure with shunt transistors. Each switch consists of two traveling-wave single-port single-throw (SPST) switches and two quarter-wavelength transmission lines. In order to further improve the insertion loss and power performance, the body floating or negative gate/body-biasing techniques are implemented. The quarter-wavelength transmission line forms an impedance transformer to transform the isolated terminal into high impedance and also the TX-RX isolation can be enhanced. The class-A PA is utilized to achieve high linearity and power gain. The five-stage cascode configuration is adopted to compensate for the conversion loss produced by the resistive mixer. using a cascode topology since such a structure provides a higher power gain and an improved reverse isolation. In order to compensate the gain degradation at higher frequencies, positive feedback is employed to enhance the effective transconductance of the common-gate transistor and to improve the gain of the cascode configuration. To achieve a broadband gain performance. The impedance-matching is composed of each driver stages designed to the different part of the band. The LNA is also designed a five-stage cascode structure in cascade to amplify the small input RF signal to minimize the overall NF of the RX chain and balance the conversion loss of the resistive mixer. The gain of the LNA is further improved through the use of gain-boosting technology. the LNA circuit employs a noise reduction approach in the first and second cascode amplifier stages to improve the NF performance. In particular, an inductor is placed in series between the common-source and common-gate stages to resonate out the parasitic capacitances and form relatively high impedance at the inter-stage node. For the mixer design, the single-ended sub-harmonic resistive mixer consisting of one transistor and four different types of filters. The transistor is constructed in a common source structure biased at zero voltage and the LO signal is fed to the gate through a band-pass filter (BPF). The time-variant channel resistance is modulated by the LO signal which mixes with the IF or RF signal at the drain to achieve up or down conversion, respectively. As a single-ended topology is adopted to achieve bidirectional operation, the port-to-port isolation performance is inevitably degraded compared to that of a double-balanced configuration. Hence, the filters in the mixer are designed to improve the isolation. In the TX mode, the transceiver has a maximum conversion gain of 2.88 dB at 94.1 GHz and a 3-dB bandwidth from 90 to 103 GHz. Moreover, the 2LO-RF leakage is less than -20 dBm over the 3-dB bandwidth. In the receiving (RX) mode, the maximum conversion gain at 94.1 GHz is 11.71 dB and the 3-dB bandwidth extends from 91 to 102 GHz. The minimum noise figure (NF) is 11.01 dB at 95.1 GHz. Finally, the total dc power consumption is 245 mW (TX:143 mW; RX:102 mW) and the overall chip size is 1.37 mm× 0.716 mm including the pads. The presented 90-100 GHz integrated bidirectional RF transceiver will be very useful for future 5G NR mmWave communication and IoT applications. Also, it can be applied to 3-D imaging radar for conceal weapon detection.