408μA/498μA 靜態電流 0.00096%/0.00166% 總諧波失真加雜訊之低失真/低電磁干擾 雙模式 D 類音頻放大器

Low-Distortion/Low-EMI Dual-Mode Class-D Audio Amplifier with 408μA/498μA Quiescent Current and 0.00096%/0.00166% THD+N

隊伍名稱 不同凡響
Marvelous Music

隊　　長 簡士雄 / 成功大學電機工程研究所

隊　　員 邱詣智 / 成功大學電機工程研究所

指導教授
郭泰豪
成功大學電機工程學系

美國馬里蘭大學電機博士，現為成功大學電機工程學系教授。
曾任晶豪科技副總經理、集新科技總經理。

研究領域
類比積體電路、混合信號積體電路、電源管理、D 類音訊功率放大器、類比/數位轉換器、數位/類比轉換器。

作品摘要

無論市場龐大的智慧型可攜式與穿戴式裝置，或是物聯網（Internet of Things，IoT）與智慧家庭裝置，使用者對於高音訊品質的需求持續提升，且各種應用在高度整合下使得電源續航力及低電磁干擾（Electromagnetic Interference，EMI）的重要性亦日趨顯著。而音頻放大器便是決定各類裝置之音訊輸出品質、功率轉換效率及電磁干擾的關鍵晶片。

高效率的 D 類放大器（Class-D Amplifier）近年已成為音訊放大器的主流，其架構上常使用閉迴路的迴圈濾波器（Loop Filter）之高迴圈增益來改善功率級失真（Power Stage Distortion），但迴授訊號中的高頻訊號會與三角波互調（Intermodulate）產生額外的脈寬調變混疊失真（PWM-Residual-Aliasing Distortion）；此外，迴路濾波器設計中存在頻帶內增益與頻帶外抑制能力間的權衡，導致傳統 D 類放大器的線性度受限。另一方面，D 類放大器常用之 BD模式的脈寬調變下，在差模與共模輸出均具有高速切換之訊號，造成不可忽視的電磁干擾；雖然德州儀器（TI）於 IEEE International Solid- State Circuits Conference論文中提出無共模 BD 模式調變（Common-Mode-Free BD，CMFBD）技術來降低共模電磁干擾，但其仍舊會因為製程變異導致元件不匹配（Mismatch）而造成不可忽略電磁干擾。

為了解決上述現存最佳技術之問題，本作品完成低失真模式（Low-Distortion Mode）/ 低電磁干擾模式（Low-EMI Mode）之雙模式 D 類音頻放大器，其系統架構如圖一所示。在低失真模式下提出創新的零相移脈寬調變混疊失真抑制技術（Zero-Phase-Shift PWM-Residual-Aliasing distortion Reduction, ZPS-PRAR），本技術突破了現存閉迴路濾波器的設計權衡，使音頻放大器不需要高切換頻率即有效降低脈寬調變混疊失真並維持抑制功率級失真的能力，此外在迴圈濾波器系統的切換頻率及運算放大器電路上亦完成最佳化來達到極低靜態電流（Quiescent Current）消耗與最高品質因數（Figure of Merit，FOM）。另一方面，在低電磁干擾模式下提出輸出共模校正（Output VCM Correction）技術，來解決現存技術中因電路不匹配而造成電磁干擾的問題，且可以省下外部電磁抑制元件的成本，就能讓裝置上的其他系統不會受到電磁干擾。

此作品實現於具成本效益的 0.5μm CMOS 製程，在低失真模式下，量測結果顯示其靜態電流達到至史無前例的 408μA、總諧波失真加雜訊（Total Harmonic Distortion Plus Noise，THD+N）為 0.00096%，如圖二中所示；與現存最頂尖的 D 類音頻放大器文獻相比，本晶片僅須有史以來最低的靜態電流消耗即達高傳真效能，品質因數亦為史上最高之 2354。而在低電磁干擾模式下，開啟共模校正技術後，其輸出共模頻譜如圖三，介於30MHz～1GHz 頻帶之最大電磁干擾抑制多達 11dB。本晶片相當適合應用於可攜式、穿戴式裝置及物聯網與智慧家庭產品，並提供雙模式的切換來符合各種應用中對於音質、靜態電流消耗、電磁干擾以及系統成本與體積等規格。

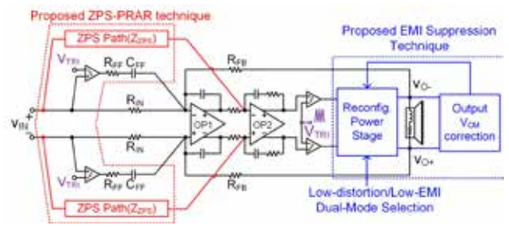

圖 1. 系統架構圖

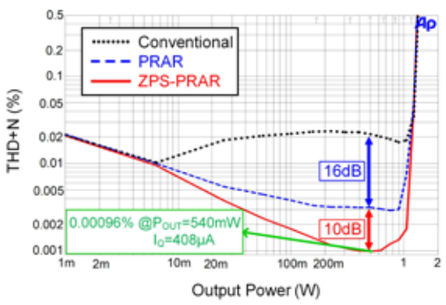

圖 2. 總諧波失真加雜訊對輸出功率量測圖

ABSTRACT

Not only in the smart portable and wearable devices with huge market but the emerging products of Internet of Things (IoT) and smart home, high audio sound quality has always been requested by user experience. In addition, battery usage time and electromagnetic interference (EMI) are getting more important when more circuits and systems are highly integrated. Among those integrated ICs, audio amplifier is the key component to determine the audio quality, power efficiency and EMI of the devices.

High-efficiency Class-D amplifier has become the mainstream structure for audio amplifier, and its closed-loop topology is usually adopted to suppress the power stage distortion by the high loop gain of the loop filter. However, the feedback mechanism introduces high-frequency PWM components, which intermodulate with the triangle wave, resulting in the PWM-residual-aliasing distortion. Due to the design tradeoff of conventional loop filters between in-band gain and out-of-band attenuation, power stage distortion and PWM-residual-aliasing distortion are difficult to be reduced at the same time, leading to a limited linearity of conventional Class-D amplifier. On the other hand, for the widely-used BD mode PWM modulation in Class-D audio amplifier, the common-mode and differential output both have high-frequency components, resulting in serious EMI issue. Even though Texas Instruments (TI) proposed Common-Mode-Free BD mode (CMFBD) to reduced EMI in IEEE International Solid- State Circuits Conference, but in reality, the EMI issue still can't be ignored with concern of circuit mismatch.

To solve above-mentioned problems, we designed and realized a dual-mode Class-D audio amplifier with low-distortion mode and low-EMI mode, and its system architecture is shown in Fig. 1. Under low-distortion mode, an innovative zero-phase-shift PWM-Residual-Aliasing distortion Reduction (ZPS-PRAR) technique is proposed. The ZPS-PRAR technique breaks the tradeoff in conventional loop filter design, making it possible to suppress both power stage distortion and PWM-residual-aliasing distortion without resorting to higher switching frequency. Furthermore, the system switching frequency and operational amplifier design are optimized to achieve ultra-low quiescent current consumption and highest figure-of-merit (FOM); on the other hand, under low-EMI mode, the output common-mode correction technique is proposed to solve the EMI problem caused by circuit mismatch. With the correction technique, there is no requirement of external EMI-suppressing components to prevent other circuits from EMI problem and the system can be more cost-efficient.

This work is implemented with cost-efficient 0.5μm CMOS technology. In low-distortion mode, the measured Class-D amplifier consumes the world's lowest quiescent current of 408μA while achieving a competitive total harmonic distortion plus noise (THD+N) of 0.00096%, as shown in Fig. 2. Compared with other state-of-the-arts, this work achieves high fidelity with the lowest quiescent current, resulting in the world's best FOM of 2354. While in low-EMI mode, the peak value of the output common-mode spectrum in 30MHz~1GHz band is greatly reduced by 11dB with the common-mode correction technique, as shown in Fig. 3. Therefore, this work has great potential to be applied in portable, wearable, IoT devices and smart home; in addition, this work provides two selectable modes to meet the different requirements of the audio quality, quiescent current consumption, EMI, system cost and size for the various applications in different products.

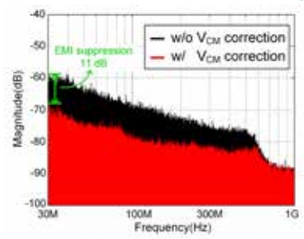

Fig.3 Output VCM spectrum with / without VCM correction