D19-073

應用於次世代400GbE乙太網路之100Gb/s四階脈衝振幅調變電壓模態傳送機搭配高效4-Tap前饋等化器及取樣相位校正技術於四十奈米CMOS製程

A 100-Gb/s PAM-4 Voltage-Mode Transmitter with Advanced 4-Tap FFE and Sampling Phase Calibration Techniques in 40nm CMOS for Next Generation 400GbE Ethernet Application

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研究領域
毫米波/射頻無線收發器、高速序列器/解序列器、鎖相迴路、時脈資料復原電路。

DESIGN GROUP D19-073

作品摘要

隨著時代的演進，許多日新月異的科技商品及服務逐漸地與網路相互結合，改變多種商業和消費者行為模式，像是近年來發展迅速的物聯網、車聯網、及雲端運算等等。而對於大企業而言，為了儲存企業營運資料，勢必需建立一個資料中心 (Data center) 來處理這些龐大的資料量，在大量湧現的雲端應用程式推動下，資料中心流量呈現飛速增長趨勢，從數據中可得知未來對於資料中心的處理資料能力的依賴及需求性，必定是逐年增加。

此次傳送機晶片是採用 TSMC 40nm CMOS 製程設計，其完整電路架構圖如圖一，傳送機傳輸型式主要則是著墨在 PAM-4 資料傳輸技術；低速部分有偽隨機二進位數列產生器，可以選擇傳送出去的訊號要是 NRZ 還是 PAM-4 的型式；第二級即是 128：16 多工器，以樹枝狀架構兩兩互相合成，其可確保訊號及時脈兩者相對應的關係；第三級為格雷碼編碼器，藉由邏輯閘重新定義其訊號編碼型式，進而降低整體傳送機的傳送誤碼率；而訊號部分，為了使最後輸出為 PAM-4 型式，在格雷碼編碼器之前，將 16 路的中速訊號之後會將 16 路的中速訊號分成最大有效位元及最小有效位元各 8 路，每個區塊皆包含有限脈衝響應產生器、8：4 多工器、單端轉雙端轉換器、4：1 多工器、前端驅動器、60 個驅動器單位細胞。

有限脈衝相應產生器能創造出不同延遲型式的平行訊號，產生出前饋等化器所需之輸入訊號，最後對高頻訊號做補償；接著是 8：4 的多工器，在此我們改變訊號的相位關係，使符合最後 4：1 多工器輸入的訊號所需；前端驅動器部分採用電阻回授架構，能降低 4：1 多工器輸出端的阻抗值，進而提升輸出的頻寬；此次提出創新的兩階段前饋等化器補償方式，在中速訊號及整個前端之間設計開關機制，控制最後前饋等化器的補償係數，能大大降低在輸出端的負載及前端部分的功率消耗，驅動器部分是採用源極串聯終端驅動器，依照電晶體與通道的阻抗值比例來決定輸出的振幅，其功率消耗低，在不同狀況下也保持在一個定值，藉此達到低功耗的目標。

本作品實現傳輸速率達到 100Gb/s 的傳送器，符合當今世代的需求。為了充分掌握國內外各大研究團隊於此領域之研究近況，我們在實作前已進行充分之文獻探索，由文獻了解各種架構並比較其優劣，從中討論如何提升傳送機之效能並透過實際 COB 量測驗證之，其各項量測及分析結果如圖二所示。

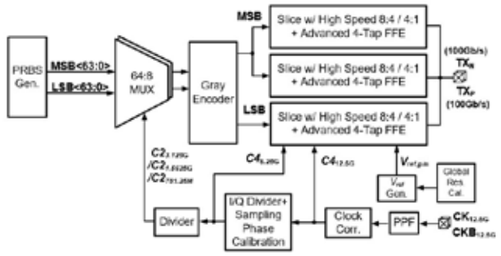

圖 1. 100Gb/s PAM-4 傳送機整體架構

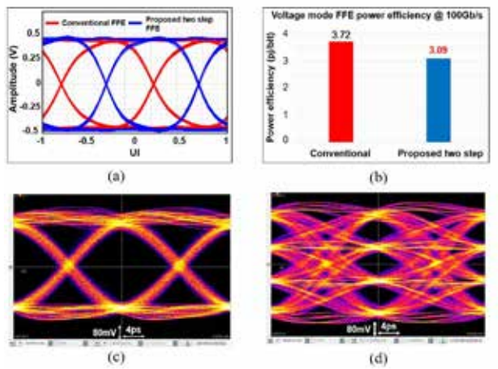

圖 2. 本企劃提出前饋等化器與傳統架構比較之(a)輸出眼圖、(b)能源效率，以及本次傳送機操作在(c)50Gb/s NRZ、(d)100Gb/s PAM-4 之量測眼圖

ABSTRACT

With the evolution of the times, many of the ever-changing technology goods and services are gradually integrated with the Internet. It changes a variety of business and consumer behavior patterns, such as the rapid development of Internet of Things, Internet of Vehicles, and cloud computing in recent years. For large enterprises, in order to store business data, it is necessary to establish a data center to handle these huge amounts of data. With the emergence of a large number of emerging cloud applications, data center traffic is growing rapidly. The data shows that the future dependence and demand for the data processing capacity of the data center must increase year by year.

The transmitter chip is designed by TSMC 40nm CMOS process. The complete circuit structure diagram is shown in Figure1. The transmission type is mainly focused in PAM-4 data transmission technology. The low-speed part has pseudo random binary sequence generator (PRBS Gen.). The signal selected for transmission is NRZ or PAM-4. The second stage is 128:16 multiplexer, which is synthesized by a dendritic structure, which ensures the corresponding relationship between the signal and the pulse. The third stage is a Gray code encoder, which re-defines its signal coding type by logic gates, thereby reducing the transmission error rate of the overall transmitter. And the signal part, in order to make the final output of the PAM-4 type, the 16-channel medium-speed signal is divided into the maximum effective bits(MSBs) and the least significant bit(LSBs) before the Gray code encoder, each of which includes a finite impulse response generator, an 8:4 multiplexer, a single-ended to double-ended converter, and 4: 1 multiplexer, front-end driver, 60 drive unit cells.

The finite pulse generator can create parallel signals of different delay types to generate the input signals required by the feedforward equalizer, and finally compensate the high frequency signals. Then the 8:4 multiplexer, where we change the phase relationship between signals to match the last 4:1 multiplexer input. The front-end driver part uses a resistor feedback architecture, which can reduce the impedance value of the 4:1 multiplexer output, thereby increasing the output bandwidth. An innovative two-stage feedforward equalizer compensation method is proposed. The switching mechanism is designed between the medium speed signal and the entire front end to control the compensation coefficient of the final feedforward equalizer, which can greatly reduce the load at the output end and the power consumption of the front end portion. The driver part uses a source series terminal driver to determine the amplitude of the output according to the ratio of the impedance value of the transistor to the channel, and the power consumption is low, and is maintained at a constant value under different conditions, thereby achieving the goal of low power consumption.

This work achieves a transmitter with a transmission rate of 100Gb/s, which meets the needs of today's generation. In order to fully grasp the research status of major research teams in this field at home and abroad, we have carried out sufficient literature exploration before implementation, and we understand the various architectures and compare their advantages and disadvantages, and discuss how to improve the performance of the transmitter and through the actual COB measurement verification. The results of various measurements and analysis are shown in Figure 2.