應用於物聯網之低功耗高速高解析類比數位轉換模組

Low-Power High-Speed High-Resolution Analog-to-Digital Conversion Module for IoT Applications

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研究領域
類比積體電路、混合信號積體電路、電源管理、D 類音訊功率放大器、類比/數位轉換器、數位/類比轉換器。

作品概述

近年物聯網市場日益增加，而國際晶片設計大廠也持續推出基於物聯網之智慧家庭及穿戴式裝置相關產品。如 Intel 開發多種模組，內含微控制器並須整合數種通訊規格如 Wi-Fi、藍牙、感測器等。物聯網整合晶片困難點之一為需整合多種規格之類比數位轉換器（Analog-to-digital converter，ADC）。此外，為延長穿戴式裝置電池壽命，低功耗成為重要發展方向。本作實現應用於物聯網之低功耗高速高解析類比數位轉換模組。此模組包含一高速低功耗 ADC 與一高解析低功耗 ADC，並提出多種創新技術，整合兩種不同頻帶之 ADC 晶片，將適用物聯網設備之系統晶片並領先目前市面上產品。兩 ADC 皆使用先進 CMOS 製程實現，以利整合至 SoC 系統。

高速低功耗六位元每秒取樣四十億次次區間式 ADC

本作實現之高速低功耗 ADC 採用次區間架構，搭配所提出之可校準式偏移誤差比較器，消除次區間參考電壓轉換所需要的趨穩時間，以實現高速運作。搭配本作提出的校正技術不僅改善比較器本身偏移誤差，亦能取代傳統參考電壓完成嵌入式參考電壓，消除電阻階梯所需之靜態電流，以實現低功耗設計。本作與現有六至八位元最佳文獻相比，在 3.6GS/s 時，有最佳的效能指標Walden FoM，為 22.7fJ/conv.-step。

高解析低功耗十六位元每秒取樣四千 / 三千萬次導管式 ADC

本作亦提出並實現具三種誤差平均技術之導管式類比數位轉換器，同時降低運算放大器有限增益及電容不匹配誤差，達到高解析度並低功耗。相關電壓位移平均技術（Averaging correlated level shifting，ACLS），平均兩個放大相位的有限運算放大器增益誤差，等效增益被提升至約為原增益的平方，且能降低放大器熱雜訊。排序電容平均（Sorted-capacitor averaging，SCA）及兩相位平均（Two-phase averaging，TPA）技術，透過平均電容不匹配誤差，達到大幅降低電容尺寸需求及簡化電容佈局複雜度，其中 SCA 適合高速而 TPA 則適合高解析。本作與現有中速高解析最佳文獻相比，是唯一能在 Nyquist 頻帶實現大於 74 dB SNDR（12 ENOB）之無校正 ADC，兩個重要效能指標 FoMW 及 FoMS 分別為 46.3/40 fJ/conv.-step 及 166.8/169.1 dB，與現有最佳文獻相比，本晶片皆為最佳。

本作提出多種創新技術，實現低功耗高速及高解析 AD 資料轉換模組，可應用於物聯網設備且性能優於目前市面上之產品。其中所使用的兩個 ADC 效能指標皆超越現有最頂尖 IEEE 論文。

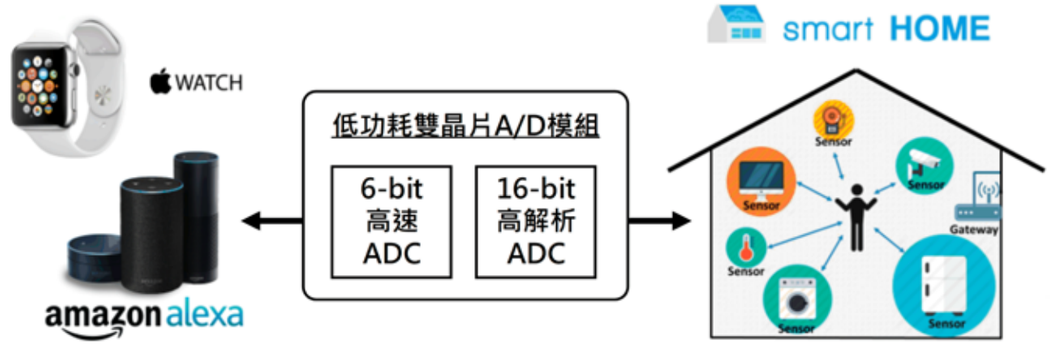

圖 1. 系統應用示意圖

ABSTRACT

Recently, the market of Internet of Things (IoT) is increasing. Thus, international manufacturers continue to introduce products for IoT applications in smart homes and wearable devices. For example, Intel developed several modules, including microcontrollers integrating several communication specifications such as Wi-Fi, Bluetooth, and sensors. One of the major challenges of IoT ICs is the need to integrate a variety of analog-to-digital converters (ADCs). Further, for wearable devices, low power consumption is essential to extend the battery life. This work implements a low-power, high-speed, high-resolution analog-to-digital conversion module for IoT applications. This module contains one high-speed, low-power ADC, and one high-resolution, low-power ADC. Several innovative techniques are proposed to combine two different frequency bands ADC chips, which is compatible for IoT devices and lead the products currently on the market. Both ADCs are implemented using an advanced CMOS process to facilitate integration into an SoC.

High-speed low-power 6-bit 4GS/s subranging ADC With the proposed offset-adjustable comparator (OAC), the high-speed low-power ADC in subranging architecture eliminates the settling time for the transition of reference voltage switching so as to realize high-speed operation. The proposed calibration technique not only mitigates the intrinsic offset of the comparators but also forms embedded reference voltage replacing conventional ones and thereby removes the static current consumption from resistor ladder for low-power design. Compared with existing 6-bit to 8-bit prior state-of-the-art ADCs, this work has the best Walden figure-of-merit (FoMW) at 3.6 GS/s, which is 22.7fJ/conv.-step.

High-resolution low-power 16-bit 40/30 MS/s pipeline ADC
This work also proposes and implements a pipeline ADC with three error averaging techniques, while reducing the finite gain and capacitance mismatch error of the operational amplifier to achieve high resolution and low power consumption. Averaging correlated level shifting (ACLS), averaging the gain error from the finite operational amplifier with two amplifying phases, the equivalent gain is enhanced to approximately the square of the original one, and also reduces amplifier thermal noise. Sorted-capacitor averaging (SCA) and two-phase averaging (TPA) techniques greatly reduce the requirement of capacitance size and simplify capacitor layout complexity through averaging capacitance mismatch errors. SCA is suitable for high speed; TPA is suitable for high resolution. Compared with the existing medium-speed high-resolution prior state-of-the-art ADCs, Only this work achieves SNDR greater than 74 dB (12 ENOB) in the Nyquist band without any calibration. The two performance indices, Walden and Schreier Figure-of-Merits (FoM), are 46.3/40.0 fJ/conversion-step and 166.8/169.1 dB, respectively.
Compared with prior state-of-the-art, this work achieves the best FoMW and FoMS.

This work proposes several innovative techniques to realize a low-power, high-speed, and high-resolution analog-to-digital conversion module for IoT applications. The performance is better than current products on the market. Furthermore, the FoM of two proposed ADCs are beyond prior state-of-the-art IEEE papers.

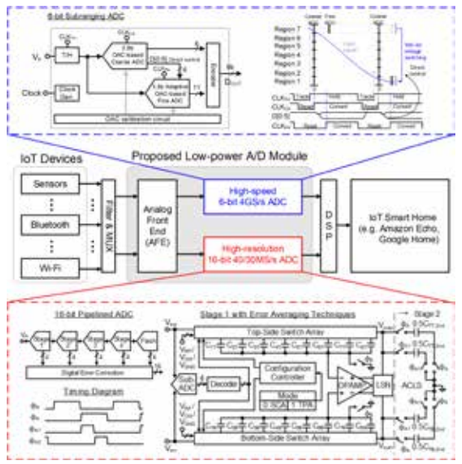

Fig.2 System block diagram