D20-002 **DESIGN GROUP**

作品名稱

具最佳迴路增益追蹤之數位鎖相迴路

Optimal Loop Gain Tracking Digital Phase-Locked Loop

隊伍名稱

敢死隊 The Death Squad

隊長

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作品摘要

在先進的單晶片系統的應用中需要許多鎖相迴路用來產生時脈或作為頻率合成器，如：有線的收發機要求有好的時域雜訊以降低資料回復電路的抖動容忍度、資料轉換器則需要克服供應電壓雜訊造成的周期時域雜訊以及處理器需要有小面積以及小功耗的時鐘。小面積的數位鎖相迴路由數位相位頻率偵測器、數位迴路濾波器、數位控制環型振盪器以及除頻器所組成，數位鎖相迴路克服了製程、電壓、溫度變異敏感的問題，且擁有小面積以及隨製程進程快速的優點，使得在量產上較類比鎖相迴路還方便；但因為整個系統幾乎都數位化，導致量化誤差變得比類比鎖相迴路嚴重，除量化誤差外，環形振盪器的相位雜訊較電感電容震盪器差而導致整體數位鎖相迴路的時域雜訊增加，而受限了數位鎖相迴路的應用；另一方面，應用於複雜數位系統的數位鎖相迴路常常需要面臨供應電壓雜訊耦合的問題。

本作品解決上述所列的數位鎖相迴路的問題：實現一個擁有最佳時域雜訊的數位鎖相迴路並且利用公式推導加入供應電壓雜訊後的最佳迴路頻寬，並且進行晶片系統中常有的供應電壓雜訊的量測。由於希望論文可以更接近量產的考量，因此本論文除了本身理論推導外，也展示了相關的模擬以及晶片量測結果。本篇論文所量測的晶片使用台灣積體電路製造股份有限公司（Taiwan Semiconductor Manufacturing Company，TSMC）所製作的 40 奈米晶片。

本作品提出的自動迴路增益校正電路使用頻譜平衡的方法，利用偵測數位相位頻路偵測器輸出的高頻與低頻的成分來對應調整迴路的頻寬，使得整體的數位鎖相迴路頻寬最後會收斂到有最小的方均根雜訊的頻寬，同時也利用數學推導以及量測證明了加入供應電壓雜訊後，所提出的鎖相迴路也可以收斂在最佳的頻寬點。在沒有供應電壓雜訊的情況下，量測到的相位雜訊在距離主頻 10 萬赫茲、100 萬赫茲、1000 萬赫茲下分別為 –90dBc/Hz、–95dBc/Hz、–101dBc/Hz，其方均根雜訊為 3.64 皮秒。在有 5 毫伏特及 30 萬赫茲的供應電壓雜訊下，使用提出的自動迴路增益電路可以使方均根雜訊值從 8.5 皮秒降到 5.1 皮秒。此數位鎖相迴路的面積與功耗分別為 0.016 平方毫米以及 1.5 毫瓦。

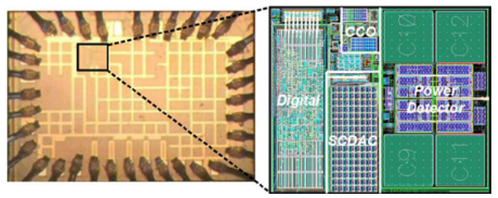

圖 1. 晶片及佈局圖

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- **研究領域：**類比 / 數位積體電路、鎖相迴路及延遲鎖定迴路、通信積體電路、混合式及射頻積體電路系統、微感測器積體電路、類比數位轉換器

Abstract

Modern system-on-chips need multiple PLLs serving as clock generators or frequency synthesizers for different intellectual properties such as wireline transmitter/receivers, data converters, and processors. For example, wireline receivers require a low jitter PLL to improve the jitter tolerance of the embedded clock and data recovery circuits, and data converters need to be immune to power supply noise to improve the period jitter, and low power and low area PLLs are required in processors. Digital PLLs (DPLLs) have been developed owing to their scalability and small area. Moreover, the DPLLs is more tolerant to the PVT variations. Digital PLLs with small are composed of a bang-bang phase-frequency detector (BBPFD), digital loop filter (DLF), digitally controlled ring oscillator, and divider. However, the ring-based VCO in DPLL has a poor phase noise performance compared with the LC-based VCO in DPLLs. Furthermore, reducing the quantization noise and the power supply noise in complex embedded digital systems is also an issue in DPLLs to achieve a better jitter performance.

This work presents a general solution to the problems mentioned above to demonstrate an optimal loop gain tracking DPLLs and also derives the optimal loop bandwidth while considering the power supply noise and gives chip measurement results to verify the derivations. We not only give the derivations but also show the completed measurement results in the hope of being mass production. The chip in this work is fabricated in TSMC 40nm process.

This work implements a digital phase-locked loop (DPLL) using the proposed adaptive loop gain controller (ALGC). The ALGC uses a spectrum-balancing technique detect the difference of the high-frequency and the low-frequency powers of the bang-bang phase-frequency detector. Then, the loop gain of the DPLL is adjusted to minimize the output root-mean-square (RMS) jitter. This DPLL is fabricated in 40-nm CMOS process and its active area is 0.016mm2. The power consumption of the DPLL is 1.5mW from a 1V supply voltage. Without the power supply noise, the measured phase noise is -90dBc/Hz, -95dBc/Hz and -101dBc/Hz at the offset frequency of 100kHz, 1MHz and 10MHz, respectively.

The integrated RMS jitter is 3.64ps, which is translated to have a figure-of-merit of -227dB. With a 5mVPP and 300kHz sinusoidal power supply noise, the RMS jitter is reduce from 8.5ps to 5.1ps by using the proposed ALGC.

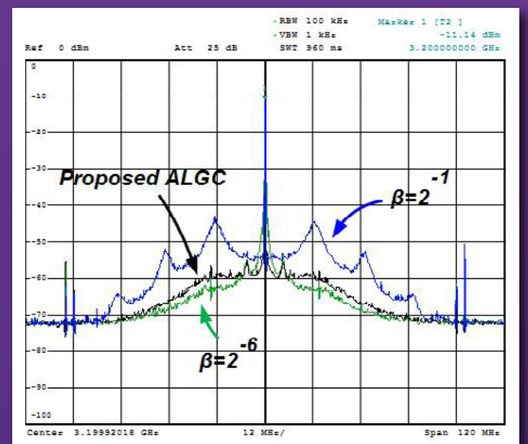

Fig. 2 Output Spectrum