D20-020 **DESIGN GROUP**

作品名稱

採用純壓控振盪式補償器且具最高效率 89% 之 2.5MHz 類電流模式時域降壓轉換器

An 1.2A $I_{LOAD,MAX}$ 89% Peak Efficiency 2.5MHz CCM/DCM Pseudo-Current Mode Buck Converter With VCO-Based PI Compensator

隊伍名稱

電源管理晶片 PMIC

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作品摘要

半導體技術隨著摩爾定律（Moore's law）演進，電晶體的尺寸不斷微縮，其工作電壓（V_{DD}）與臨界電壓也隨之降低。為了實現節能且體積小等發展的趨勢，本研究嘗試將時域（Time–domain）控制模式導入電源管理晶片（Power management IC）中，其優點為具類數位訊號（Digital–like signal）但沒有量化誤差（Quantization error），因此非常適合隨製程演進。

本作品所採用之時域模式降壓轉換器（Buck converter）方塊圖如圖 1 所示。電壓（V_e）經由電壓－時間轉換器（Voltage–time conversion）轉成時間資訊，再透過時域處理器（Time domain processing）所產生的時脈推動功率電晶體，最終可透過系統之負回授，將輸出電壓（V_{OUT}）鎖定在預設的參考電壓（V_{REF}）上。

本作品提出之電路架構結合了多種習知電路的架構與技術，取其所長結合而成，相較於過往的作品，有以下特點：

1. 提升時域模式降壓轉換器之轉換效率。傳統時域模式的切換頻率（Switching frequency）皆大於 10 MHz，如此一來將造成在輕載待機時，有較大的切換損耗（Switching loss）。因此，本作品設法將操作頻率降至 2.5 MHz，並提出降低設計複雜度之技巧。
2. 僅採用壓控震盪器（VCO）與高通濾波器（High–pass filter）實現 PI 補償。電壓透過高通濾波器將可產生微分之效果，接著透過重複利用的 VCO 即可同時實現 P 與 I 補償。如此一來，就不需要再設計電壓控延遲線（VCDL）元件，大幅降低低頻下的電路設計複雜度。
3. 可利用被動元件實現高通濾波器做補償，也可大幅降低控制電路之功率消耗。
4. 為了延長多媒體設備之待機時間，本作品也採用零電流偵測電路（Zero current detector），以避免逆電流發生，使其在長期待機操作時，可以更加省電。

本作品為採用純壓控振盪式 PI 補償器之 2.5MHz 類電流模式時域降壓轉換器，其晶片圖如圖 2 所示。此晶片採用台積電 180nm 製程，並且為第一個僅採用電壓控制振盪器實現 PI 補償，同時具有低頻率高轉換效率之時域電壓轉換器電路，其內部無使用任何類比放大積分補償器與類比數位轉換器，且具有類數位控制之優點，包含可低電壓操作、高製程延展性且降低設計複雜度。除此之外，此架構之控制電路面積非常小，因此具低成本。

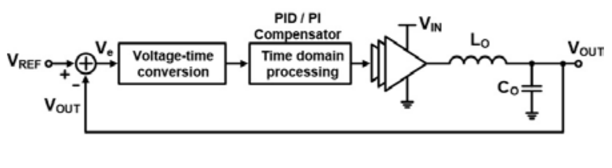

圖 1. 時域模式降壓轉換器方塊圖

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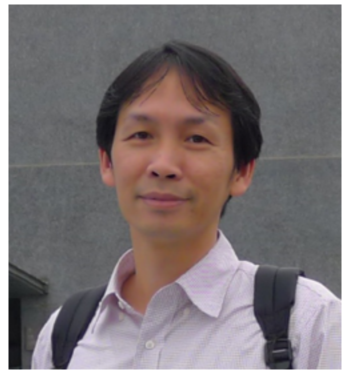

- 美國加州大學洛杉磯校區電機博士，現為臺灣大學電機工程學系教授。曾任職於博通（Broadcom Corporation）參與類比 / 射頻 / 混合訊號電路設計，並開發無線傳輸系統。
- **研究領域：**生醫應用高能量效率無線通訊晶片、電源管理晶片、應用於 PLL 與 Delta–Sigma ADC 之混合信號電路設計技術、感測器與生醫應用類比訊號處理電路

Abstract

Time-domain (TD) signal processing has been applied to switched-mode dc-dc converters recently. The converter output voltage (V_{OUT}) is transformed to TD information as the processing variable, which operates like digital signals but without quantization error. Furthermore, the digital-like nature allows TD circuits to operate at a lower supply voltage (V_{DD}), which leads to lower power consumption. Various TD power converters with PID/PI compensators have been reported, as conceptually depicted in Fig. 1. The prior works operate at higher switching frequency (f_{sw} > 10 MHz) for small form factor and fast transient. However, this is at the cost of decreased power efficiency. Lowering f_{sw} can lead to better efficiency, but the design complexity of VCDL increases as the switching period becomes longer.

Another issue of TD (or phase-domain) operation in a TD power converter is the phenomenon of harmonic locking. If a PD is adopted in the controller, during load transient. The V_{OUT} may be locked to a wrong value. This is due to that a conventional PD is simply a SR latch. The PD is not able to provide the direction of the phase difference from its input signals; namely, it lacks the frequency information. If the f_{sw} is sub-harmonically locked to a wrong frequency, and V_{OUT} is also incorrect.

To address the aforementioned design issues, a pseudo-current mode (PCM) VCO-based buck converter is proposed in this work. In the PI compensator, the proportional element is implemented as a differentiator followed by a VCO. Hence, VCDL is no longer required. Next, to avoid harmonic locking, phase-frequency detector is adopted. Finally, to improve the efficiency at light load, zero-current detector is realized to enable the converter to enter DCM operation.

This work presents a 2.5MHz CCM/DCM pseudo-current mode buck converter with a VCO-based PI compensator. The proposed PI compensation with inductor current sensing eliminates the power-hungry voltage-controlled delay line (VCDL) that is required in a conventional time-domain compensator and reduces the design complexity. To avoid har-monic locking during large load transient, phase-frequency detector (PFD) is employed. Finally, a zero-current detector (ZCD) is adopted to prevent the power loss in light-load operation. The proposed chip is fabricated in TSMC 180-nm CMOS process, as shown in Fig. 2. With a 3.3V input and 1.2V output, the peak efficiency of 89% is achieved. The maximum load current is 1.2A.

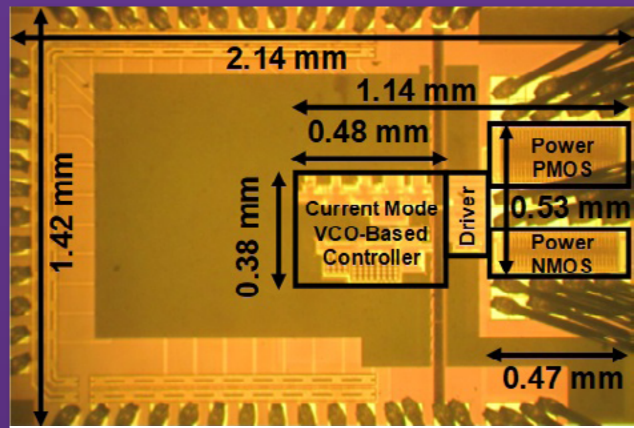

Fig. 2 Chip micrograph