D22-052

具備原位容錯能力 RISC-V 處理器與全集成切換式電壓調節器之 28 奈米高能效微處理器系統單晶片

An Energy-Efficient Microprocessor System-on-Chip Featuring an In-Situ Error-Resilient RISC-V Core and an Embedded Switching Voltage Regulator in 28-nm CMOS

隊伍名稱　特級雙份鮪魚上腹
　　　　　Double Premium Otoro
隊　　長　吳秉宸 / 臺灣大學電子工程學研究所
隊　　員　陳瑋廷 / 臺灣大學電子工程學研究所

指導教授

劉宗德　臺灣大學電機工程學系

臺灣大學電機工程學士、碩士、加州大學柏克萊分校電機工程博士，現為臺灣大學電機工程學系副教授。曾於聯發科技參與無線通訊電路與系統設計，亦曾為柏克萊無線研究中心成員、於比利時校際微電子研究中心從事半導體電路技術研究。

研究領域

高能效電路與系統設計

作品摘要

能量使用效率是物聯網（Internet of things，IoT）邊緣設備最重要的關鍵性能指標。這是因為物聯網設備必須要廣泛部署在無線連接的環境中，並提供各種新興應用，例如智能監控、生物識別、非接觸式人機介面等。而這些邊緣裝置內包含了多個由微處理器控制的無線收發器、傳感器/轉換器和輸出介面模組。並且隨著對功能的需求不斷成長，單個設備上的微處理器數量也隨之增加。此外，邊緣設備的功率預算高度受到電池或能量擷取效率的限制。因此，提高微處理器的能量使用效率是在邊緣設備上實現更複雜、更進階的應用的關鍵。

為了滿足此要求，如圖一所示，我們提出了一個系統單晶片設計，該設計集成了一個RISC-V微處理器和一個全集成的開關電容穩壓器，並實作於28奈米CMOS製程。該設計在CMOS技術中實現了最先進的能量延遲乘積（energy-delay product，EDP），且包含了以下特色：

1. 使用了具備原位錯誤檢測和糾正（error detection and correction，EDAC）功能之正反器，其能夠容忍製程、電壓與溫度變異，並且其錯誤糾正過程可以直接在電路層級完成，不需要重新執行處理器指令。此外，與文獻中的其他解決方案相比，該設計不需要測試校準，這極大地有利於量產。
2. 使用了一種具備容錯能力的靜態隨機存取記憶體（SRAM）介面，以克服傳統EDAC技術難以和SRAM緊密耦合的缺點。此技術可以進一步增強容錯能力，並且是一個非侵入式的技術，高度支援傳統的設計流程。

3. 將一個高效能的電壓轉換穩壓器完全集成在晶片上，以最大限度地減少PCB佔用的面積和電壓轉換損耗。該電壓轉換穩壓器採用了一個名為雙速搜尋的調節算法，和動態導通損耗最小化技術，可減少輸出電壓的壓降，同時最大限度地提高轉換效率。
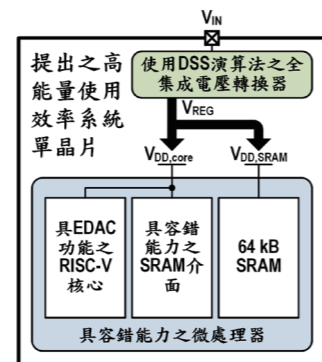
圖一 具備原位容錯能力 RISC-V 處理器與全集成切換式電壓調節器之高能效微處理器系統單晶片設計

Abstract

Energy efficiency is the most critical key performance index for the Internet-of-things (IoT) edge devices. This is because the IoT devices are widely distributed, deployed, or equipped in the environment with a wireless connection to the network to provide a variety of emerging applications, such as intelligent monitoring, biometrics, contactless human interfacing, or even their combinations. In addition, multiple microprocessor-controlled components of wireless transceivers, sensors/transducers, and output devices are integrated on the edge devices to realize those applications. Moreover, the number of microprocessors on a single device increases along with the growing demands on functionality. Furthermore, the power budget of the edge devices is highly constrained by the battery or the harvesting sources. As a result, improving the energy efficiency of the microprocessors is the key to enabling more advanced applications with higher complexity on the edge devices.

To fulfill the energy efficiency requirement, as shown in Fig. 2, we present a system-on-chip (SoC) design consisting of a RISC-V microprocessor design and a fully integrated switched-capacitor voltage regulator (SCVR) in the 28-nm CMOS process. The proposed system achieves a state-of-the-art energy-delay product (EDP) in the CMOS technology. Such advanced results are enabled by following features:

1. In-situ error detection and correction (EDAC) flip-flops (FF) enable the tolerance to the PVT variations, and no instruction replay is required for correction. With this feature, the timing margin in the sub- or near-threshold region can be significantly minimized. In addition, the proposed design does not require post-silicon calibration, which greatly benefits mass production.
2. An error-resilient technique for static random-access memory (SRAM) interfaces is proposed to overcome the weakness of the conventional in-situ EDAC technique. This feature can further enhance the capability of the error-resilience of the proposed design in a non-invasive manner, and this technique is compatible with the conventional cell-based design flow.
3. An SCVR is fully integrated on the chip to minimize the PCB footprint and conversion loss. This SCVR features a regulation algorithm of dual-speed search (DSS) and a dynamic conduction loss minimization technique to reduce the voltage droops of the output voltage while maximizing the conversion efficiency.
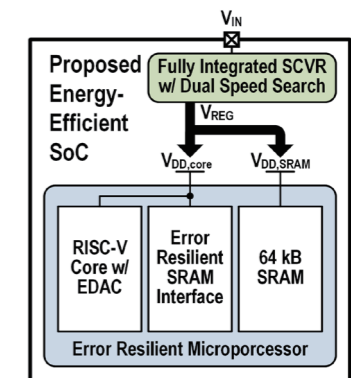

Fig. 2 An energy-efficient microprocessor system-on-chip featuring an in-situ error-resilient RISC-V core and an embedded switching voltage regulator