D22-064

一個 103fJ/b/dB, 10-26 Gbps 高頻寬高雜訊容忍度之雙迴路巢狀接收機

A 103 fJ/b/dB, 10-26 Gbps Receiver with a Dual Feedback Nested Loop CDR for Wide Bandwidth Jitter Tolerance Enhancement

隊伍名稱　抗噪達人
Noise-cancelling Expert
隊　　長　黃宇平 / 陽明交通大學電子研究所
隊　　員　劉曜嘉 / 陽明交通大學電子研究所

指導教授

陳巍仁　陽明交通大學電子研究所

交通大學電子研究所博士，現為陽明交通大學電子研究所暨電機工程學系教授。曾任交通大學電子研究所所長、IEEE 固態電路學會臺北分會主席。

研究領域

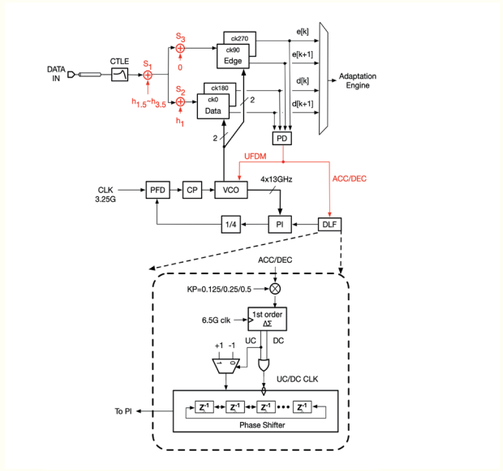
混合信號積體電路、高頻電路、通信積體電路

作品摘要

圖一為系統架構，為了要能適應極高的輸入衰減訊號會先經過線性等化器並且使用決策等化器做後續最佳化。為了要讓功耗以及硬體得到最簡化的結果，本作使用邊際等化技巧降低對額外的振幅優化演算法的依賴。透過後續的邊際跟資料取樣結果使用解多工器（demux）降低取樣速率到數位端去做後處理，包含適應性演算法和偏移校正等。為了降低時脈相位回復電路的延遲，本作使用客製化的類比投票器，此投票器可以有三種判斷狀態包含領先，落後和平衡。此外透過高速相位移位暫存器控制相位內差器（phase interpolator），為了更進一步降低延遲此移位暫存器操作在1/4 速率作為時脈資料迴路電路的同步時脈。巢狀式迴路要操作再更高的頻寬，為了不要和時脈相位鎖定電路的頻寬互相影響降低穩定度。此設計我們大約操作在100MHz除了穩定的度考量之外，因為多相位產生器實際上是環相振盪器的輸出因此高頻寬也有助於對於輸出雜訊做抑制的功用。為了減少相位內差器跳動產生的量化雜訊，本作使用128相位內差半速率的時脈，先經過電流邏輯除二電路在使用雙端轉單端的電路做大訊號的轉換，增加電路的操作穩定度跟降低功耗使用。

最後本作提出的高速調變機制（UFDM ultra-fast direct modulation）讓整體巢狀迴路的設計缺點包含延遲效應跟振盪器雜訊都可透過此技術進一步較正。且因重複使用相位偵測器的輸出並沒有多出額外的高速電路。

等化器使用類比以及決策等化器同時運作達到32dB 損耗規格，為了更近一步提升功耗表現，本作完全使用邊際雜訊收斂演算機制，此機制不需額外的振幅偵測機制因此可以減少時脈樹（clock tree）的產生，實驗證明此等化器搭配時脈回復電路可以達到BER 1e-15，因此適用IEEE應用範圍。與現有技術相比，它顯示出比傳統雙環CDR節省2倍的功率。考慮到可容忍的通道損耗，整個接收器表現出迄今為止最好的FoM，即103 fJ/b/dB。



圖一 系統架構圖

Abstract

A nested loop CDR (NL-CDR) incorporates only a single PR inside the PLL. They minimize the number of employed PI, and remedy the difficulties of high-speed multi-phase clock distribution. The loop delay of the PLL impedes high frequency jitter tolerance of NL-CDR. To overcome this drawback, this project proposes a dual feedback nested Loop CDR (DF-CDR).

Fig. 1 shows the receiver architecture. To tolerate up to 32 dB channel loss, it is composed of a CTLE followed by data and edge decision feedback equalizers (DFE) with a DF-CDR. A half rate, 2X oversampling PD is utilized in this design to have a higher ISI resilience over its baud rate counterparts. The DF-CDR is based on a 13 GHz PLL with a 3.25 GHz reference, which is available from the global clock source in the transceiver. The sampling phases of the half-rate receiver are derived from the quadrature output phases of VCO directly, which are adjusted through rotating PI’ s output phase. In contrast to the conventional NL-CDRs, the PD output provides an additional ultra-fast direct modulation (UFDM) path to the VCO in this design. It accelerates the phase tracking capability as well as reducing the loop latency of CDR and resembles an auxiliary derivative control path to complement the low-pass tracking of the PI path.. It minimizes the loop latency to avoid phase margin and jitter tolerance degradation around the CDR bandwidth. The PLL features a wide loop bandwidth of 200 MHz to facilitate VCO in band noise suppression. It greatly relaxes the phase noise requirement of the VCO, and thus benefits from a significant power saving in broad band and low jitter sampling clock generation.

Fig. 2 shows the simulated waveforms before and after equalization. Under a 32 dB loss channel, the data eye at the receiver input is totally closed without CTLE and DFE. By applying zero forcing algorithm, the jitter histograms are more concentrated at the edge DFE output compared to that at the CTLE output. Moreover, the eye opening at the data DFE output is 240mV, which has about four times improvement with 0.5 UI timing margin.

A Nested CDR based Receiver with PID controller is presented. The direct modulation jumps over the loop latency limited PI path and modulate VCO for faster response and enhance the stability. By applying PRBS-7 test pattern, the jitter tolerance is 0.55UIpp at 60MHz. The jitter tolerance is improved by 0.15 UI by activating the UFDM path of the CDR. Considering the tolerable channel loss, the whole receiver demonstrates the best FoM of 103 fJ/b/dB as are reported to date.

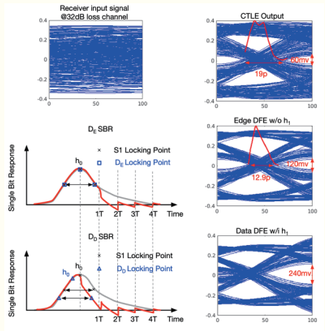


Fig. 2 Equalization