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一個無參考時脈且具有背景自我校正技術之相位雜訊量測電路

A Reference-Free Phase Noise Measurement Circuit with Background Self-Calibration

隊伍名稱　多的是你不知道的事
There Are Many Things That You Don't Know
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研究領域

混合信號積體電路、高頻電路、通信積體電路

作品摘要

隨著製程微縮，系統操作速率與資料吞吐量越高，意味著位元時間的縮短，因此系統對時脈抖動的要求日趨嚴苛。有鑑於此，一個內建於晶片的相位雜訊量測電路在未來將不可或缺。我們提出一個無須參考時脈且具有背景自我校正技術的相位雜訊量測電路。

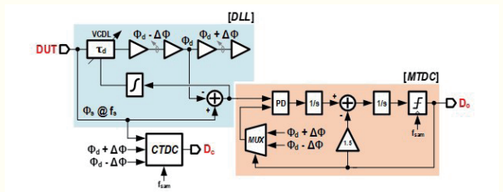
近年來實現內建於晶片上的相位雜訊量測電路大致為兩種主流，分別是延遲線鑑別器（Delay Line Discriminator，DLD）和時間至數位轉換器（Time-to-Digital Converter，TDC）：

1. 對於DLD，此架構的好處是無須額外的參考訊號源來觀察待測訊號（Device under Test，DUT）。利用比較DUT經過延遲單元前後的資訊，萃取出其相位雜訊。然而，由於其內部的類比電路如低雜訊放大器（LNA）以及混頻器（Mixer）需要額外的增益校正機制（Gain Calibration），才能正確的量測雜訊大小。另外，由於輸出形式為微小的類比電壓，不僅在量測時需要頻譜分析儀和高頻探針，也容易受到外界環境的干擾，影響結果的準確度。
2. 對於TDC，此架構利用三角積分轉換器，將DUT的相位抖動轉換成數位碼，解決DLD架構需要高端儀器及易受環境干擾的問題。然而卻需要額外的參考訊號源，且量測雜訊的靈敏度受限於參考訊號源的雜訊水平。

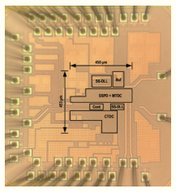
本作品結合兩架構的優點並解決上述問題，無須額外的參考訊號並以數位碼的形式量化相位雜訊。更提出以校正用TDC （Calibration TDC，CTDC）使電路能在背景監控並修正雜訊的量化間距，除了降低電路性能受製程、電壓及溫度變異的影響，也能放寬TDC的解析度。

系統如圖一所示，由一延遲鎖定迴路（DLL）及兩組TDC組成。藉由DLL和CTDC將DUT與延遲後的訊號鎖定，並產生量測雜訊的依據給MTDC，MTDC再依此轉換DUT的抖動大小為數位碼。我們只需對兩組TDC的數位碼做快速傅立葉轉換（FFT），即可回推DUT相位抖動的絕對量值。

本晶片採用TSMC 28nm CMOS製作。在打入6.4GHz的待測訊號下，此系統在頻率偏置1MHz處擁有-118 dBc/Hz的相位雜訊靈敏度。而在抖動量值的測試中，此電路可解析出275.4fs的相位抖動，與儀器量測值262.8fs相比僅有4.8%的誤差。綜觀目前已提出的數位式相位雜訊量測電路，本作品不僅省去額外的參考訊號源，且具備背景自我校正的能力，並達到至少三倍以上的抖動量測解析度及最高的準確度。



圖一 系統架構圖



圖二 晶片照相圖

Abstract

With the scaling of silicon technology, the operating speed and data throughput of systems become higher than before. It implies that bit time is getting shorter and the requirement for phase noise/jitter will become increasingly stringent. In view of this, a phase noise measurement (PNM) circuit built in chip is bound to be essential in the future. We present a reference-free PNM circuit with background self-calibration.

Several attempts for high-sensitivity PNM circuits have been reported previously. One is Delay Line Frequency Discriminator. It measures the phase noise through a delay line based frequency discriminator. The cycle jitter is translated to voltage through a mixer or a phase detector with its output in analog form, i.e. analog PNM (A-PNM). The fidelity of the spot noise density and jitter amplitude counts on external low noise amplifier and analog to digital data converter, and requires extensive off-line calibration of all the analog parameters. On the contrary, another is digital PNMs, which proposed jitter measurement through on-chip time to digital converters (TDC). They are more robust against PVT variations by converting noise spectrum into digital codes directly. However, a spectrally clean reference is required for the on-chip TDCs. Besides, the quality of reference signal would fundamentally limit the achievable noise floor of the PNM circuits.

In contrast to the prior art, we proposes PNM technique through cycle jitter measurement using an on-chip TDC, which is reference-free and thus not limited by the noise floor of the reference clock. The noise information is digitized on chip. Both the timing jitter and spot noise density can be fully processed digitally without resort to an extra high-end LNA and ADC. The timing basis of the on-chip TDC is background self-calibrated without a reference clock. The fidelity of the PNM output is verified in accordance with the measurement results by using a spectrum analyzer. Fig. 1 shows the system architecture of the proposed PNM circuit, which is composed of a DLL-based frequency discriminator coupled with a main 2nd order continuous time ΔΣ TDC (MTDC). Additionally, an auxiliary calibration ΔΣ TDC (CTDC) is incorporated to calibrate the quantization step ($\pm \Delta \phi$) of the MTDC in the background. The noise spectrum density can be derived from Fast Fourier Transform (FFT) result of the two TDC outputs. Therefore, the proposed PNM circuit provides a convenient way to measure the phase noise/jitter of a signal under test by using logic analyzer.

This work is fabricated in TSMC 28nm CMOS process. Fig. 3 shows the measurement results of phase noise sensitivity at 1 MHz offset (refer to 6.4 GHz carrier) is -118 dBc/Hz. In Fig.3, for broadband noise measurement, our design also features the finest resolution of 275.4 fsrms. Compared with the measurement results by spectrum analyzer, the discrepancy is less than 4.8%.

In summary, we propose a phase noise measurement circuit that is reference-free, background self-calibrated, and capable of digitizing the power spectral density of phase noise directly. Its measurement result demonstrates at least 3X finer jitter resolution with highest accuracy compared to the prior art.

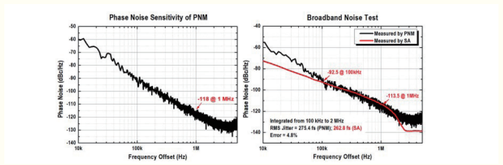


Fig. 3 Noise measurement performance of proposed system