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達成超快速且超節能並具備多種節電模式之低電壓SRAM的多模式協作輔助電路

Coordinated Multi-Mode Assist Circuits to Achieve Ultra-High Operating-Speed and Energy-Efficiency for Low-Voltage SRAM Equipping Power-Saving Modes

隊伍名稱 | 超越良馬對 Beyond the Dialogue on Excellent Steeds
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研究領域

低功耗與高速數位電路、SoC設計。

作品摘要

在南宋時期，抗金名將岳飛曾以「良馬對」來闡述戰馬的選擇之道。這段典故強調：「良馬有兩類，一種擅長持久奔馳，一種擅長迅速爆發，卻難以兼備兩者。」我們的設計理念正是從這個思想出發，並進一步突破既有限制。因此，我們的隊伍名稱「超越良馬對」，意味著我們的目標不僅是遵循岳飛對良馬的標準，而是進一步超越它，定義一個全新的「良馬之道」。在岳飛時代，人們只關注速度與耐久力之間的取捨，卻未曾思考「如何在高速運作的同時，達到極致的能效？」這正是我們的設計理念與傳統觀念的差異。我們的設計不僅要「跑得快」，還要「跑得遠」，更要「省草料」。

當今半導體靜態隨機存取記憶體 (Static Random-Access Memory, SRAM) 的設計，經常面臨速度、操作功耗、待機功耗的三大挑戰：

1. 若只追求高操作速度 → 會增加面積與操作功耗，影響能效。
2. 若只追求低操作功耗 → 則可能導致操作速度下降，影響效能。
3. 若只追求低待機功耗 → 則可能犧牲操作速度，影響整體設計的優化。

為了解決這三大難題，本作品提出「良馬之道」：嶄新的低電壓SRAM設計策略。透過多模式協作輔助電路 (Coordinated Multi-Mode Assist Circuits)，本設計可動態調節SRAM在讀寫、待機、深度睡眠與關機模式下的輔助電壓，實現同時兼具速度、能效、低耗電的低電壓SRAM設計。本作品以22-nm 0.5-V 256-Kb SRAM作為技術展示的載具，相比於同樣儲存量且為當今最好的0.5-V SRAM設計，達到以下指標：

1. 工作頻率提升6.25倍
2. 能耗降低91%

3. 待機功耗節省83%
4. 面積縮小73%
5. 額外具備深度睡眠和關機模式

本設計不僅是現代物聯網場景中的「千里良馬」，更是一匹融合速度、效能與節能的戰馬，為低電壓SRAM開創革新格局。這正是我們「超越良馬對」所提出的良馬之道：「快若疾風、靜若安眠、千里持久，冠絕天下！」

	ISSC-17 [9]	ISSC-18 [16]	TCASII-20 [1]	TVI-SI-21 [7]	TCASII-18 [15]	TCASII-23 [18]	ISSC-22 [17]	TCASII-17 [8]	This work
Technology	28-nm Bulk CMOS	28-nm Bulk CMOS	28-nm Bulk CMOS	28-nm FDSOI	28-nm FDSOI	28-nm FDSOI	55-nm Bulk CMOS	28-nm Bulk CMOS	22-nm Bulk CMOS
Capacity	256 Kb	32 Kb	32 Kb	16 Kb	128 Kb	128 Kb	8 Kb	256 Kb	256 Kb
Access bits	64	32	8	8	64	32	16	64	32
	Type	DRC-6T	customized 6T	univocal 6T	9T	7T	7T+NDR	13T	standard 6T
Bit cell	Cell area (normalized to standard-6T)	1×	n.a.	1.3×	(including overhead for VDD control)	1.65×	2.16×	2.95×	n.a.
	Write	NBL	WT boosting	2 VDD sources with read/write control	Data-aware	WT & WW1 boosting + body biasing*	FDDP + negative WW1*	3T write port	WT-CVDD
	Read	-	n.a.	3T read port	3T read port	4T read port	4T read port	4-bit local BL	BLUD
	Standby	n.a.	n.a.	n.a.	n.a.	tail buffer + body biasing*	Dual source voltage + NDR + FDDP	HVT transistors in 6T	Threshold power-gating
	Deep sleep	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	Peripheral: Support cut-off Cell array: NR-CVSS
	Shutdown	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.
f_{max}				15 MHz* @ $E_{ao}=0.41$ V	7.5 MHz*	15 MHz* @ $E_{ao}=0.24$ V	64 MHz* Read: 4.3 MHz Write: 4.6 MHz	20 MHz (1)	125 MHz (6.25)
Energy/access-bit	0.5 V or @ E_{ao}	n.a.	n.a.	167.9 fJ @ 0.41 V	840 fJ	36 fJ* @ 0.24 V	24.5 fJ* Read: 18 nJ Write: 31 nJ	468 fJ (1)	81.9 fJ (0.18)
Energy/total-bit				41 aJ @ 0.41 V	410 aJ	17.68 aJ* @ 0.41 V	6 aJ* Read: 21.3 nJ Write: 25.5 nJ	114 aJ (1)	10 aJ (0.09)
f_{min}				400 MHz* 200 MHz* @ $V_{ao}=0.7$ V	50 MHz*	15 MHz*	120 MHz* Read: 21.3 nJ Write: 25.5 nJ	150 MHz (1)	305 MHz (2.03)
Energy/access-bit	0.6 V or @ V_{ao}	n.a.	n.a.	n.a.	1.35 pJ*	n.a.	29.5 fJ* Read: 41.4 nJ Write: 84.7 nJ	94.2 fJ (1)	90.1 fJ (0.96)
Energy/total-bit				n.a.	659 aJ*	n.a.	7 aJ* Read: 47.9 fJ Write: 84.7 fJ	23 aJ (1)	11 aJ (0.48)
SEI Power/bit	0.5 V	n.a.	n.a.	n.a.	n.a.	2.5 pW*	36 pW* @ 0.4 V	229 pW (1)	39 pW (0.17)
DS Power/bit	0.5 V (not available)	n.a.	n.a.	n.a.	n.a.	5.25 pW*	0.04 pW*	343 pW (1)	62 pW (0.18)
SD Power/bit	0.5 V	n.a.	n.a.	n.a.	n.a.	n.a.	n.a.	12 pW	17 pW
								10 pW	14 pW
Macro Area (mm ²) (Normalized) (percentage of array)				0.028 (0.56)	n.a.	0.161* (0.81)	0.075* (0.38)	0.041 (0.36)	0.397 (1.00)
PPAs (D-nm ² /mm ² /bit)				183 @ 0.41 V	n.a.	56* @ 0.24 V	18* @ 0.5 V	904 @ 0.5 V	42 @ 0.5 V

* Measured with off-chip CVSS. * Simulation results of redesigned DRC-6T SRAM macro with CSVG* from outside of the SRAM. * SRAM macro area (process)/capacity. * Estimation. * Energy/access-bit > normalized-area. * Not include power and area of some assist voltage generators.

表一 比較表。

Abstract

During the Southern Song Dynasty, the renowned general Yue Fei illustrated the philosophy of selecting warhorses through his famous “Dialogue on Excellent Steeds.” This historical allusion emphasizes: “There are two types of excellent steeds: one excels in enduring long distances, while the other is superior in swift bursts of speed, but combining both traits is nearly impossible.” Inspired by this philosophy, our design concept seeks to surpass traditional limitations. Consequently, our team’s name, “Beyond the Dialogue on Excellent Steeds,” represents our ambition to go beyond Yue Fei’s original definition and establish a novel “Philosophy of the Excellent Steed.” While ancient wisdom emphasized only the trade-off between speed and endurance, it never addressed the critical question: “How can we achieve both high-speed operation and ultimate energy efficiency simultaneously?” This distinction marks our innovative approach compared to conventional thinking. Our goal is not merely to be “fast” or “enduring,” but also “highly energy-efficient.”

With the continuous scaling of Integrated Circuit (IC) manufacturing processes, chip integration levels have significantly increased. As a result, reducing power consumption and improving energy efficiency have become critical challenges for IC designers. From a system perspective, completing tasks quickly and transitioning circuits into standby, deep sleep, or even power-off modes are essential power-saving strategies. This demands that all sub-circuits be equipped with appropriate operational modes to satisfy system-level requirements. Among all components within a system-on-chip (SoC), static random access memory (SRAM) consumes the most power. SRAM is a full-custom circuit and already difficult to design. When combined with the requirements for energy efficiency, power reduction, and support for multiple modes, it presents an even greater challenge for designers:

1. Solely pursuing high operational speed → increases chip area and power consumption, negatively impacting energy efficiency.
2. Solely targeting low operational power → reduces operating speed, degrading performance.
3. Solely focusing on low standby power → sacrifices operating speed, complicating overall design optimization.

To address these challenges, this work proposes the “Philosophy of the Excellent Steed”: an innovative design strategy for low-voltage SRAM. Through the proposed coordinated multi-mode assist circuits, the assist voltages of SRAM are dynamically adjusted during read/write, standby, deep sleep, and shutdown modes, thereby achieving high speed, high energy efficiency, and low power consumption simultaneously. Implemented and demonstrated through a 22-nm 0.5-V 256-Kb SRAM test chip, our design significantly outperforms the current state-of-the-art 0.5-V SRAMs of equivalent storage capacity, achieving the following metrics:

1. 6.25x higher operating frequency
2. 91% lower energy consumption
3. 83% standby power reduction
4. 73% smaller area
5. Additional deep sleep and shutdown modes supported

This design embodies a modern “excellent steed,” effectively blending high speed, high energy efficiency, and low power consumption, thus pioneering a new paradigm for low-voltage SRAMs in IoT scenarios. This precisely defines the “Philosophy of the Excellent Steed” proposed by our “Beyond the Dialogue on Excellent Steeds” team: “Swift as the gale, quiet as deep sleep, enduring as a thousand miles, and unmatched across the world!”

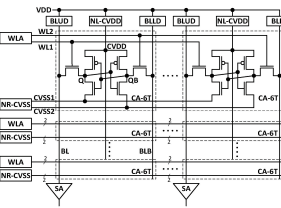


Fig. 1 Circuit of one bank of proposed LV SRAM.

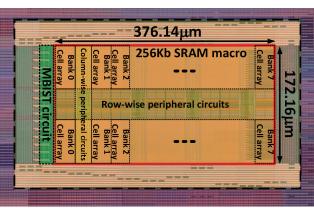


Fig. 2 Die photo of test chip.