D25-026

一個應用於中長距離傳輸之106.25-Gb/s PAM-4接收器於28奈米製程

A 106.25-Gb/s PAM-4 Receiver for Medium-Reach Application in 28-nm CMOS

隊伍名稱｜高情商領航者 EQ Pioneers

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研究領域

超高速有線通訊傳收機、光纖通訊介面、鎖相迴路及其應用、毫米波無線通訊傳收機。

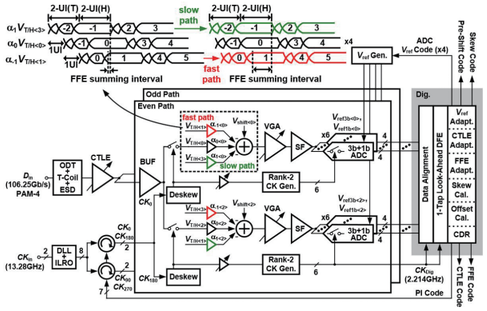
作品摘要

近年來，隨著人工智慧（AI）、5G、物聯網（IoT）等技術的快速發展，以及雲端運算需求的大幅增長，資料中心（Data center）的擴張與升級變得愈加迫切。資料中心通常由大量伺服器機架組成，每個機架內包括伺服器、儲存系統、防火牆和加速器等元件。隨著資料中心運算需求的增加，各主機之間的資料傳輸速率也要求更高效的乙太網路連接，從而推動了乙太網路技術規格的升級。

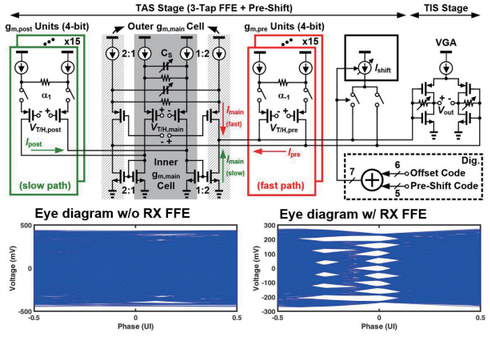
為了有效支援資料傳輸，每個機架頂部均設置了交換器（top-of-rack switch），並依據連接距離選擇銅纜或光纖將各主機與交換器相連。傳統的交換器設計通常採用可插拔模組（pluggable module），通過將交換器晶片的電訊號轉換為光訊號，再透過光纖傳輸，並在另一端將光訊號轉換回電訊號，以便進一步處理。然而，這種傳統的可插拔模組使用離散元件（discrete components），導致不僅成本較高，體積也較大。

由於傳統插拔模組所帶來的高損耗和延遲問題，下一代乙太網路交換器的解決方案是採用共封裝光元件（co-packaged optics，CPO）。這種技術藉由光訊號的傳輸以減少通道的損耗，因此可以大幅降低電氣晶片（EIC）的功耗及延遲，並且可以將八個通道以上的EIC與光晶片（PIC）一同藉由矽中介層（silicon interposer）一同整合在一個矽基板上，達到2.5D晶片的整合，也為往後矽穿孔（TSV）技術的3D晶片整合系統做準備。因此將單通道EIC的電氣頻寬達到100Gb/s甚至200Gb/s以上，便可使單一模組資料率達800Gb/s或1.6Tb/s，也為下一世代的資料傳輸提供了嶄新的實現方式。

本作品於二十八奈米製程下提出一符合光共同封裝技術應用之接收端（RX），其架構包含連續線性等化器（CTLE）、可變增益放大器（VGA）、三抽頭前饋等化器（FFE）及一抽頭推測性決策回授等化器（speculative DFE），並搭配分時多工類比數位轉換器（TI ADC）來解碼1+0.5D訊號，使得接收端在不需要任何發射端的等化器（EQ）補償下，補償通道損耗為21.2dB，資料傳輸速度達到單通道106.25Gb/s，誤碼率低於1E-12，接收端能源效率為2.06pJ/b，完整且創新的EQ技術也為將EIC單通道傳輸速率提升至200Gb/s提供可能的解決方案。



圖一 接收器架構圖。



圖二 FFE+VGA電路圖及眼圖。

Abstract

In recent years, the rapid advancement of technologies such as AI, 5G, and the IoT, along with the growing demands in cloud computing, has made the expansion and upgrading of data centers increasingly urgent. A typical data center is composed of numerous server racks, each containing servers, storage systems, firewalls, and accelerators. As computing demands grow, the overall data throughput requirements between servers in data centers are increasing, thereby driving the evolution of Ethernet standards and necessitating more efficient high-speed interconnects.

To support efficient data transmission, each rack is typically equipped with a Top-of-Rack switch. Depending on the interconnect distance, copper cables or optical fibers are used to connect servers to the switch. Traditional switch designs rely on pluggable optical modules that convert the electrical signals from the switch ASIC into optical signals for fiber transmission and reconvert them to electrical signals at the destination. However, these pluggable modules are built from discrete components, resulting in higher cost, larger physical footprint, and increased signal loss and latency.

To address the high insertion loss and latency inherent in traditional pluggable optics, the next-generation Ethernet switch architecture adopts CPO. This technology leverages optical signaling to minimize channel loss, significantly reducing the power consumption and latency of the EIC. Furthermore, it enables the integration of more than eight high-speed SerDes channels with PIC on a single silicon substrate using a silicon interposer, achieving 2.5D integration. This architecture also lays the groundwork for future 3D IC integration using TSV. By increasing the electrical bandwidth up to 100 Gb/s or even 200 Gb/s per lane, individual CPO modules can achieve total data rates of 800 Gb/s or 1.6 Tb/s, providing a breakthrough approach for next-generation data transmission.

This work proposes a CPO-compatible RX implemented in a 28-nm CMOS process. The RX architecture includes a CTLE, a VGA, a 3-tap FFE, and a 1-tap speculative DFE. In addition, a TI ADC is adopted to decode the 1+0.5D PAM-4 signal. The RX compensates the channel loss of 21.2 dB without any TX equalization. Designed and fabricated in 28-nm CMOS, the RX achieves a BER of < 1E-12 at 106.25 Gb/s with 2.06-pJ/b energy efficiency. The complete and innovative equalization architecture provides a possible solution of 200-Gb/s EIC designs for ultra-high-speed SerDes applications in the future.

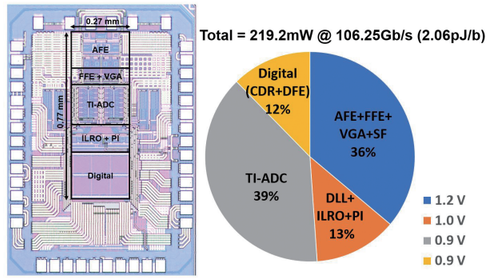


Fig. 3 Chip photo and power breakdown.

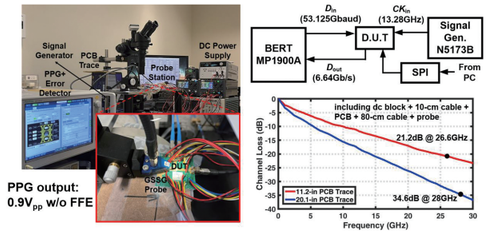


Fig. 4 Testing setup.