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適用於分速率多重接取通訊系統之高吞吐量巨量多使用者多天線偵測器

A High-Throughput Massive MU-MIMO Detector for Rate-Splitting Multiple Access Communication Systems

隊伍名稱｜暢通無阻 No Block

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研究領域

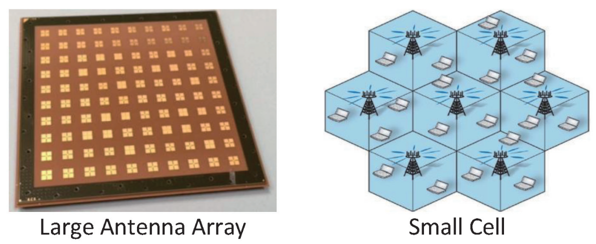
AI晶片設計、基頻通訊積體電路、生醫訊號處理晶片設計。

作品摘要

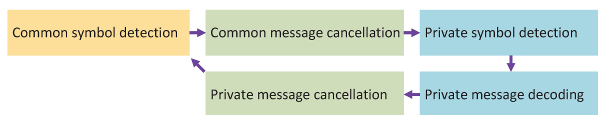
未來的無線通訊系統隨著行動裝置日新月異的發展，對吞吐量的需求日益增加。面臨下世代通訊，多使用者多輸入多輸出（MU-MIMO）系統採用了多種先進的通訊技術以滿足吞吐量需求，例如圖一的大型天線陣列搭配高頻率載波和小蜂巢式基地台。儘管這些技術旨在提升資料傳輸速率，但它們同時也為傳輸通道帶來一些不利的條件，如空間相關性、多使用者干擾、通道狀態資訊不準確，可能使資料傳輸速率低於理想通道的情況。現今的分空間多重接取（SDMA）在這些不利通道下的錯誤率表現就差於分速率多重接取（RSMA）1.9至5.8dB。

本作品實作適用於分速率多重接取的巨量多使用者多天線偵測器。圖二為所提出之偵測演算法流程，改良自文獻中傳統的偵測方法。兩者的差別有二，其一移除共同訊息解碼，其二加入私人訊號干擾消除並進行迭代。移除共同訊息解碼並搭配跳過迭代技巧可降低整體運算延遲高達93%，進行迭代可彌補前者帶來的SNR損失，迭代三次後SNR損失為極小的0.1dB。本作品的硬體方塊圖如圖三。

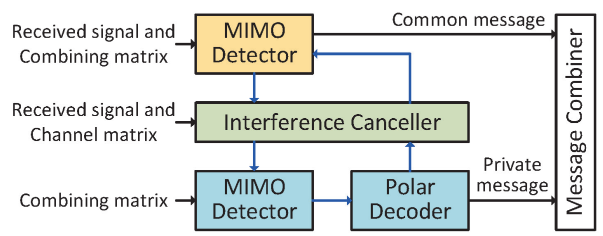
本作品在硬體最佳化方面有許多改善，包括乘法架構設計和多精度複數乘法器達成47%連續乘法延遲縮短與36%乘法器面積降低。極化碼解碼器以低複雜度運算單元降低37%面積，且為管線化設計，支援部分更新解碼技巧。干擾消除器利用部分平行化之預編碼計算縮短30%干擾消除延遲。晶片以40nm製程下線，支援256×32 MIMO規模、最高256-QAM調變與128位元極化碼解碼功能，操作在200MHz下達到最高吞吐量6.4Gbps，僅消耗功耗142mW。吞吐量為先前分空間多重接取偵測器作品之3.3倍，能量效率則為2倍。



圖一 下世代通訊應用情境。



圖二 RSMA偵測之工作流程。



圖三 RSMA偵測器方塊圖。

Abstract

As mobile devices continue to evolve rapidly, future wireless communication systems face increasing demands for higher throughput. In response to next-generation communication needs, multiuser multiple-input multiple-output (MU-MIMO) systems employ a variety of advanced communication technologies to meet these throughput demands, such as higher-frequency carriers, large antenna arrays, and small-cell base stations. While these technologies are designed to enhance transmission data rates, they also introduce unfavorable channel conditions, including spatial correlation, multiuser interference, and inaccurate channel state information, all of which may result in actual transmission data rates falling short of the ideal channel capacity. The existing space-division multiple access (SDMA) performs worse than rate-splitting multiple access (RSMA) under these unfavorable channel conditions, with a gap in error rate performance of 1.9 to 5.8 dB.

This work implements a massive MU-MIMO detector for RSMA systems. The proposed detection algorithm improves upon traditional methods in the literature. There are two key differences: (1) the removal of common message decoding, and (2) the addition of private message interference cancellation. The workflow then becomes iterative. Removing common message decoding along with an iteration skipping technique reduces overall latency by up to 93%. The iterative detection and decoding process helps compensate for the resulting SNR loss, which is reduced to a negligible 0.1 dB within three iterations. The system architecture of the proposed RSMA detector is shown in Fig. 4.

The proposed RSMA detector includes several hardware optimizations, such as a matrix-vector multiplication architecture design and a dual-precision complex-valued multiplier, achieving a 47% reduction in successive multiplication delay and a 36% reduction in multiplier area. The polar code decoder utilizes low-complexity processing units to reduce area by 37%, and it features a pipelined design that supports partial decoding update technique. The interference canceller employs partially parallelized computations for precoding to reduce interference cancellation delay by 30%. Fig. 5 shows the die photo. This chip is fabricated in 40 nm CMOS technology. It supports a 256×32 MIMO configuration, up to 256-QAM modulation, and 128-bit polar decoding function, achieving a maximal throughput of 6.4 Gbps at 200 MHz with a power consumption of 142 mW. The throughput is 3.3 times higher than previous SDMA detectors, and the energy efficiency is doubled.

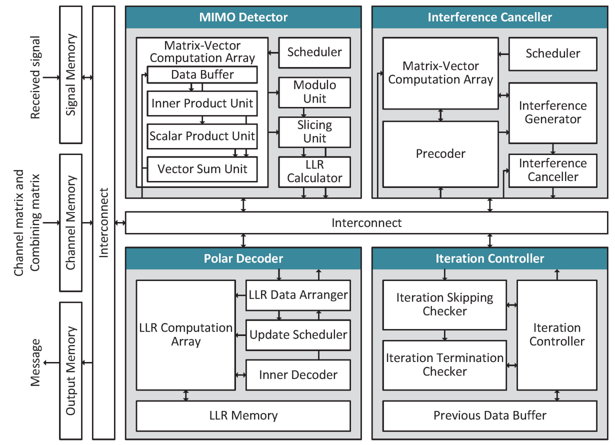


Fig. 4 System architecture.

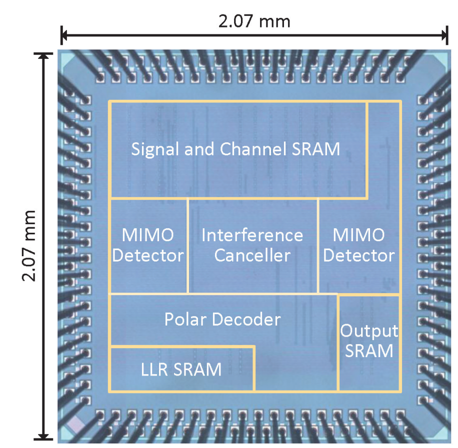


Fig. 5 Die photo.